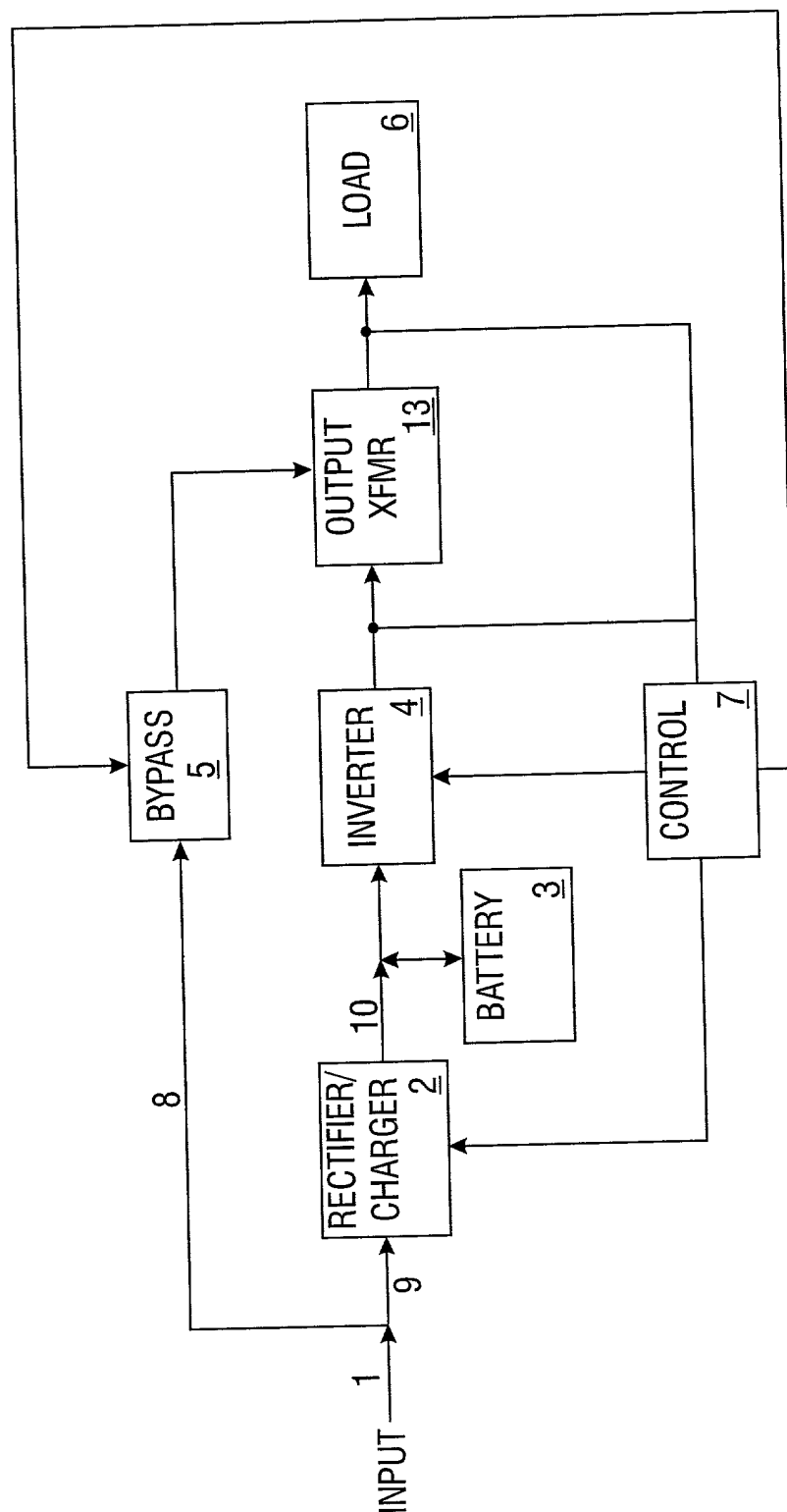


**CONCLUSIONS**



**FIG. 1**







```
graph TD
    NETWORK[NETWORK 31] --- RS232
    MODEN[MODEN 30] --- RS232
    PC[PC 29] --- RS232
    RS232 --- MICRO[MICRO MONITOR INTERFACE 19]
    SITESCAN[SITESCAN 32] --- RS485
    RS485 --- MICRO
    MICRO --- NAC[NAC]
    NAC --- WEB[WEB BROWSER]
    MICRO --- CAN
    CAN --- COTROL[COTROL BOARD 15]
    MICRO --- KEYPAD[KEYPAD 27]
    MICRO --- LCD[LCD 28]
    MICRO --- MULTI[MULTI-MODULE 1-6]
```

The diagram illustrates the system architecture with the following components and connections:

- NETWORK 31**, **MODEN 30**, and **PC 29** are connected to the **MICRO MONITOR INTERFACE 19** via an **RS232** bus.
- SITESCAN 32** is connected to the **MICRO MONITOR INTERFACE 19** via an **RS485** bus.
- The **MICRO MONITOR INTERFACE 19** is connected to a **NAC** (Network Access Controller), which in turn connects to a **WEB BROWSER**.
- The **MICRO MONITOR INTERFACE 19** is connected to a **COTROL BOARD 15** (Control Board) via a **CAN** (Controller Area Network) bus.
- The **MICRO MONITOR INTERFACE 19** is also connected to a **KEYPAD 27**, an **LCD 28** (Liquid Crystal Display), and **MULTI-MODULE 1-6**.

A circular black ink stamp from the Office of Intellectual Property (OIPE). The text "OIPE" is at the top, "JCS" is at the top right, "AUG 01 2002" is in the center, and "PATENT &amp; TRADEMARK" is at the bottom.





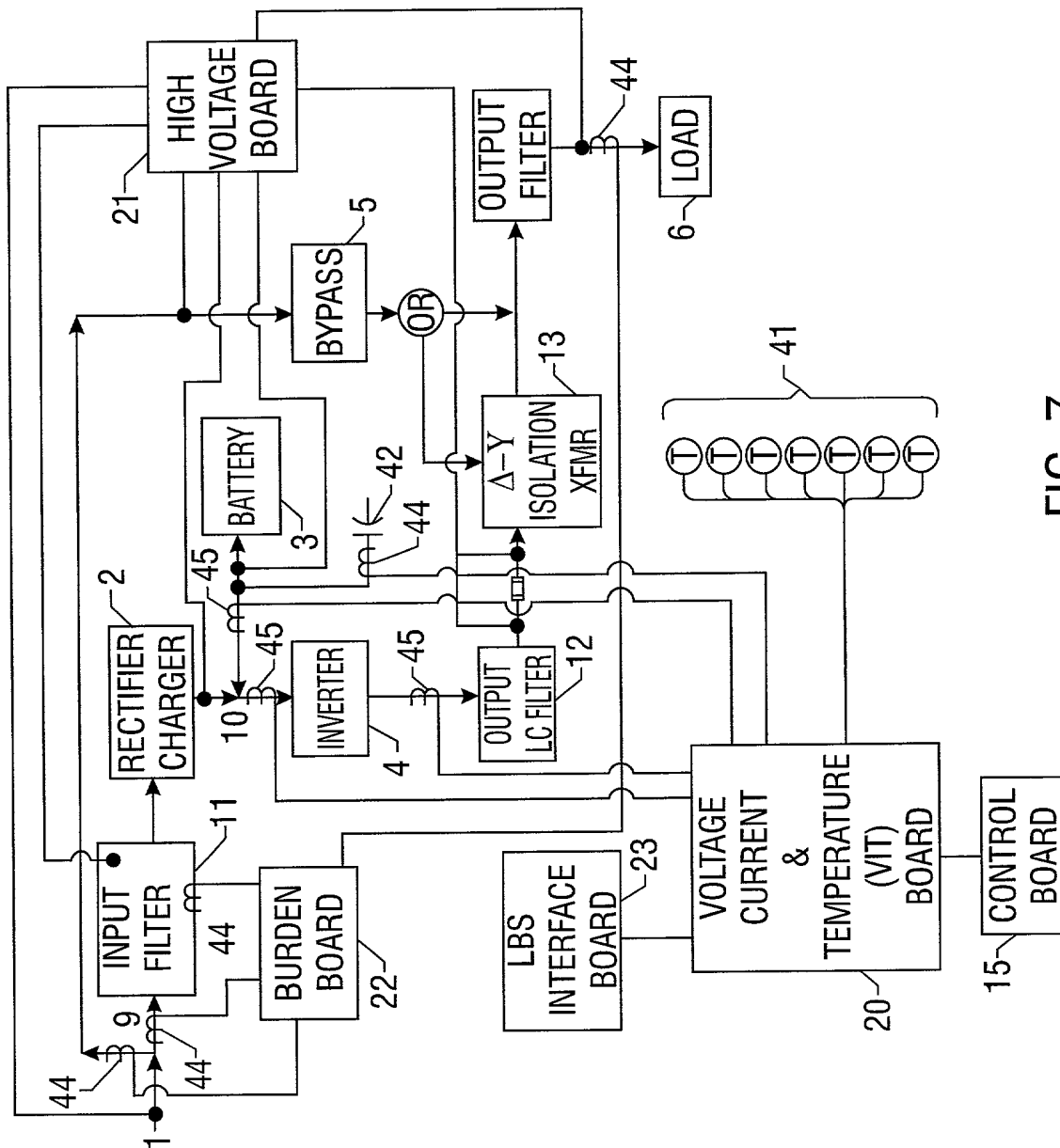


FIG. 7

2007-08-01 10:00:00

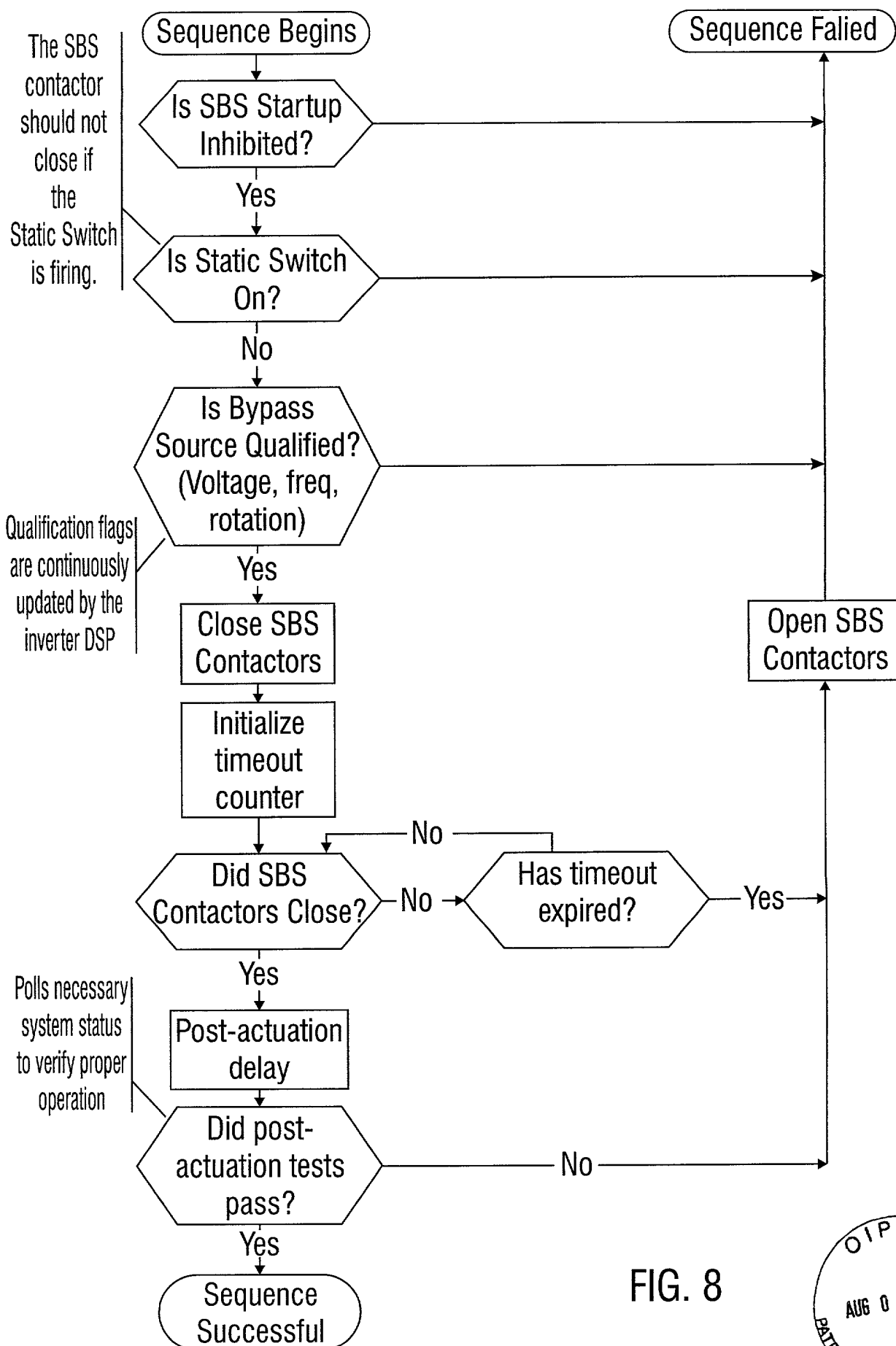


FIG. 8





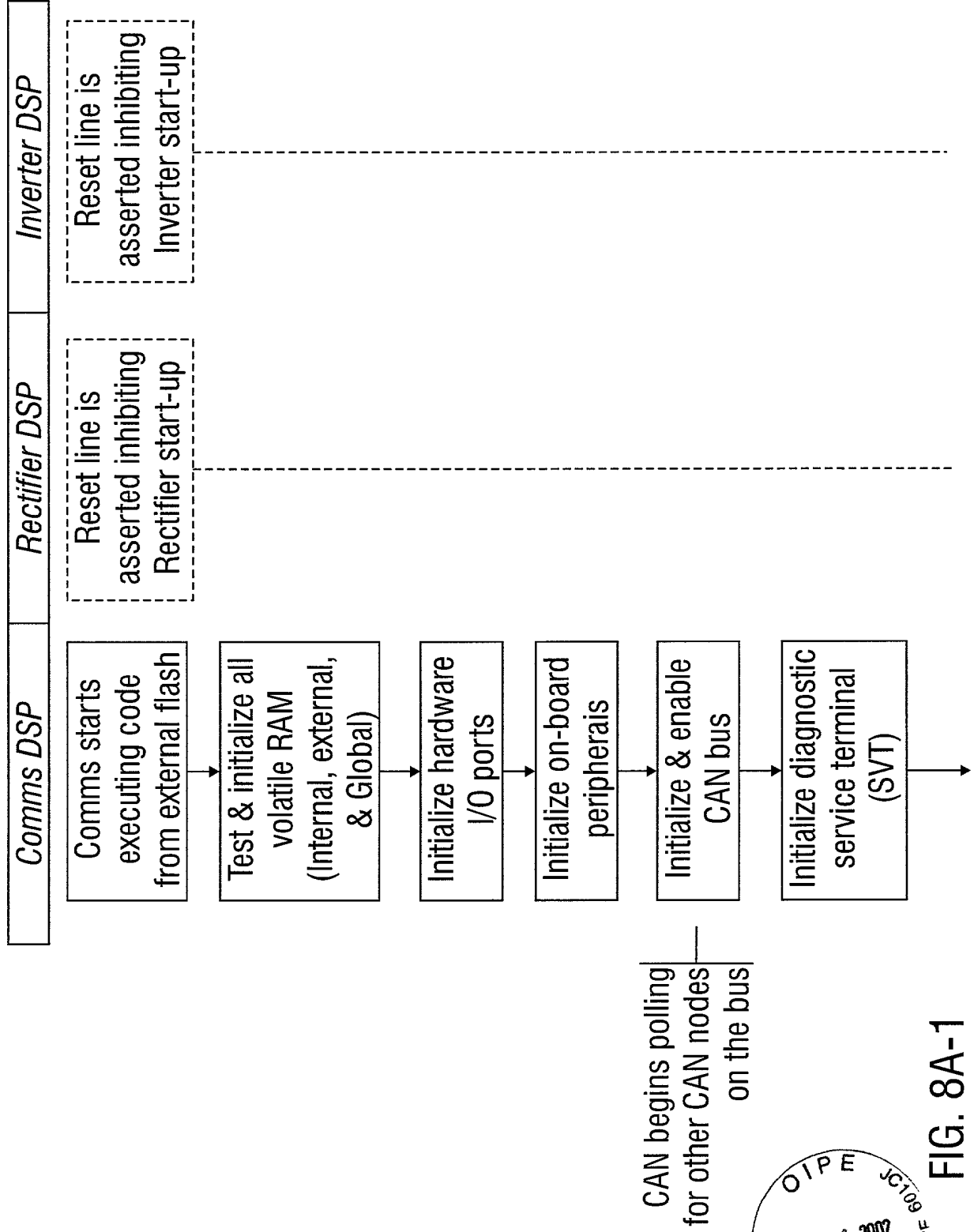
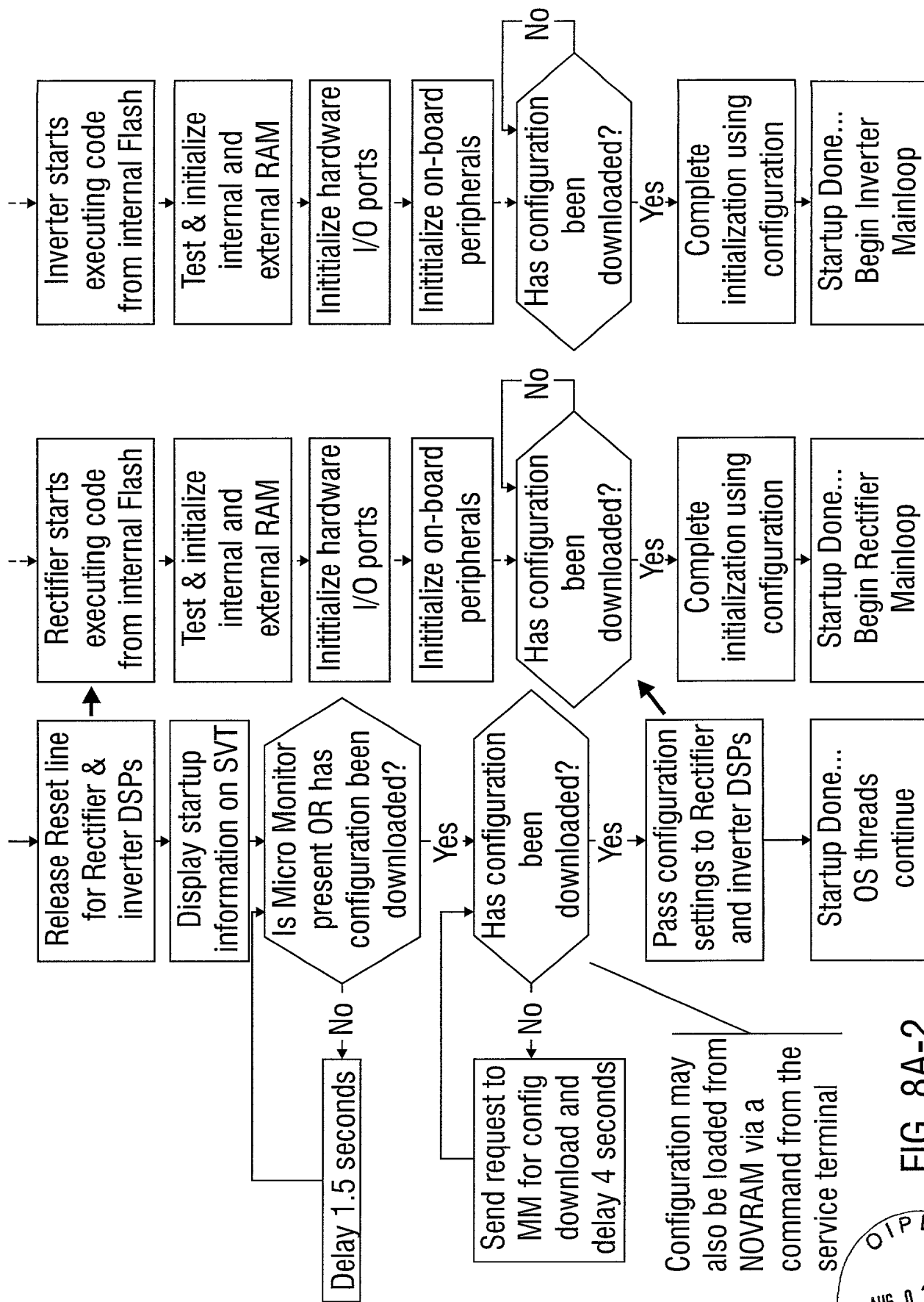


FIG. 8A-1



Configuration may also be loaded from NOVAM via a command from the service terminal

FIG. 8A-2



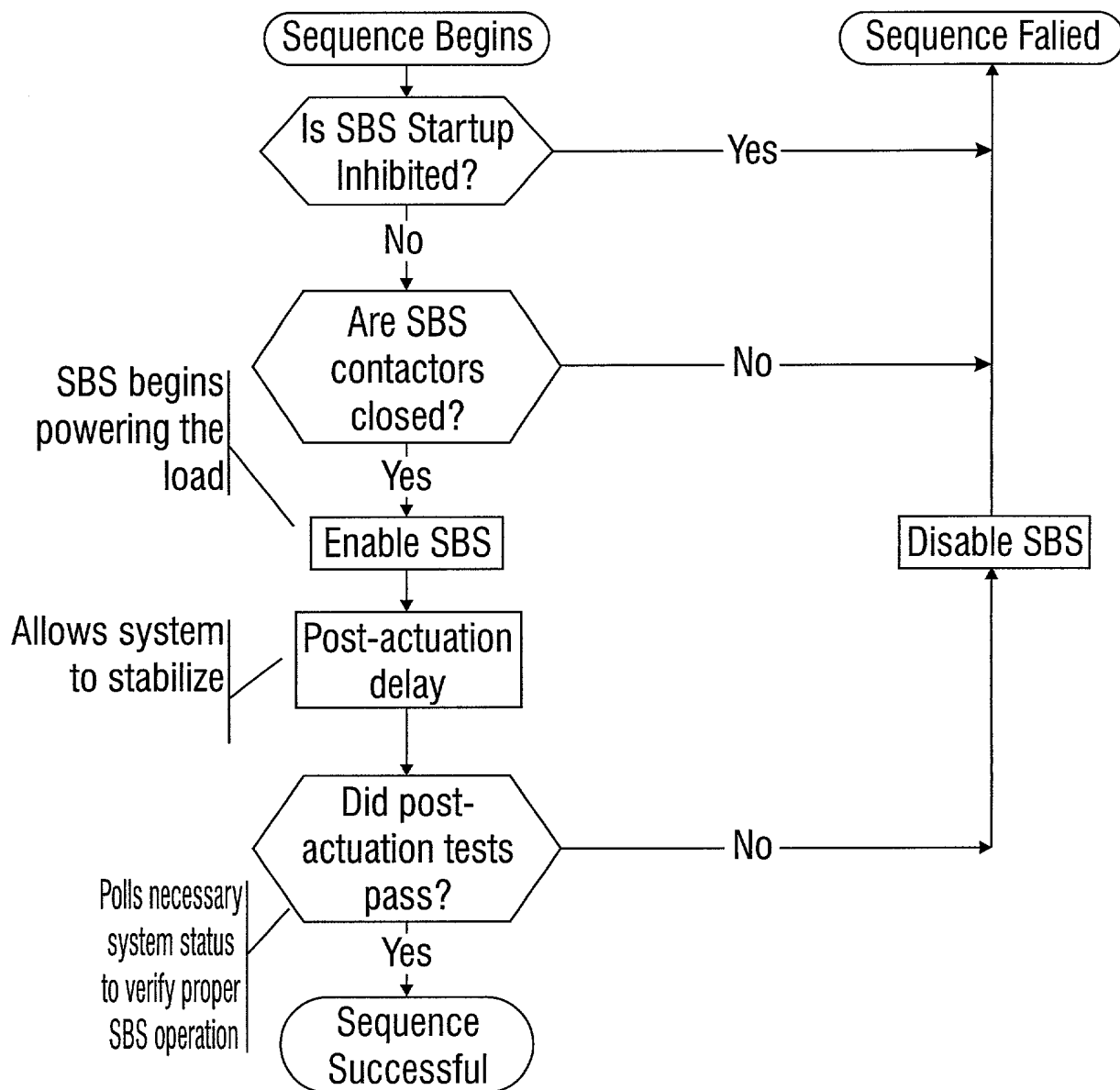


FIG. 9



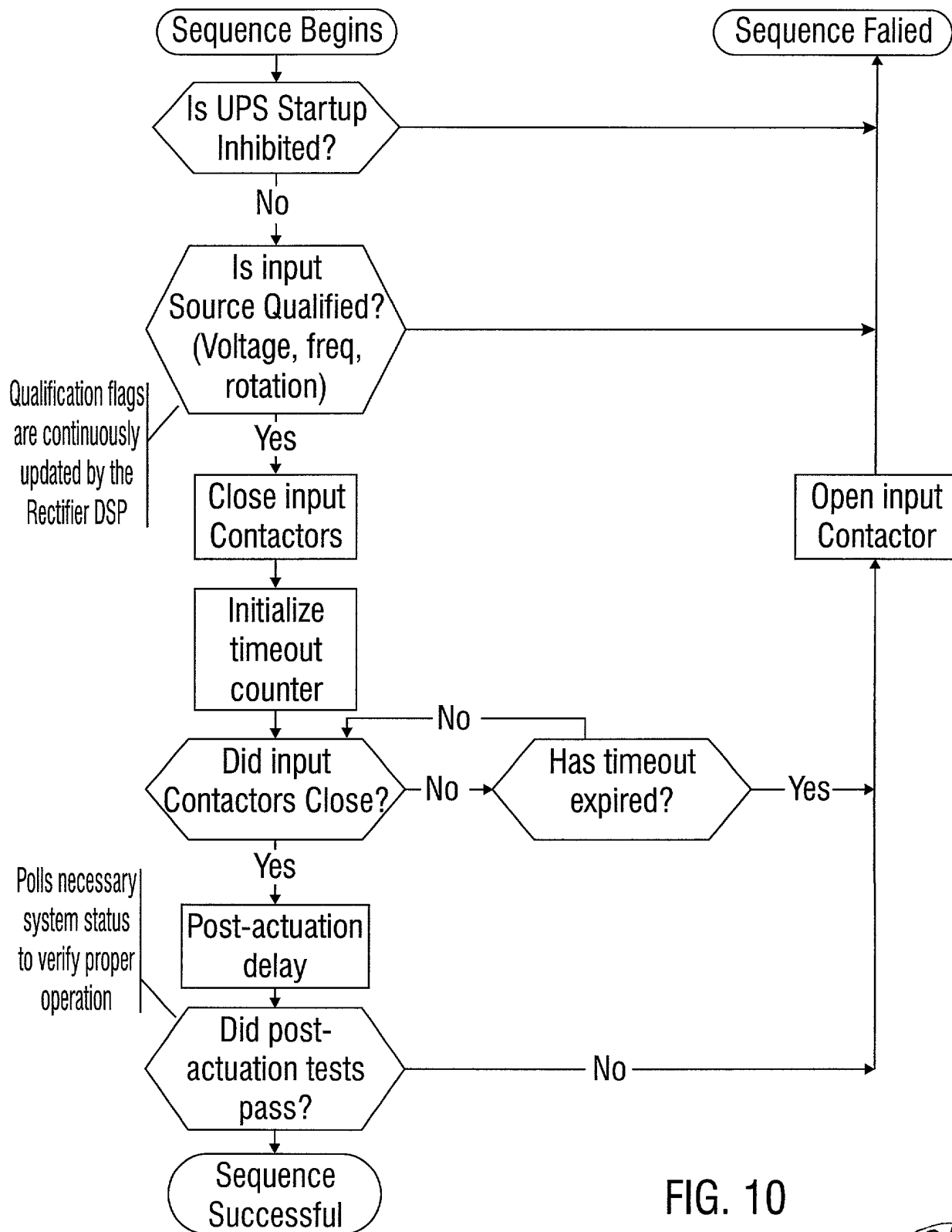


FIG. 10



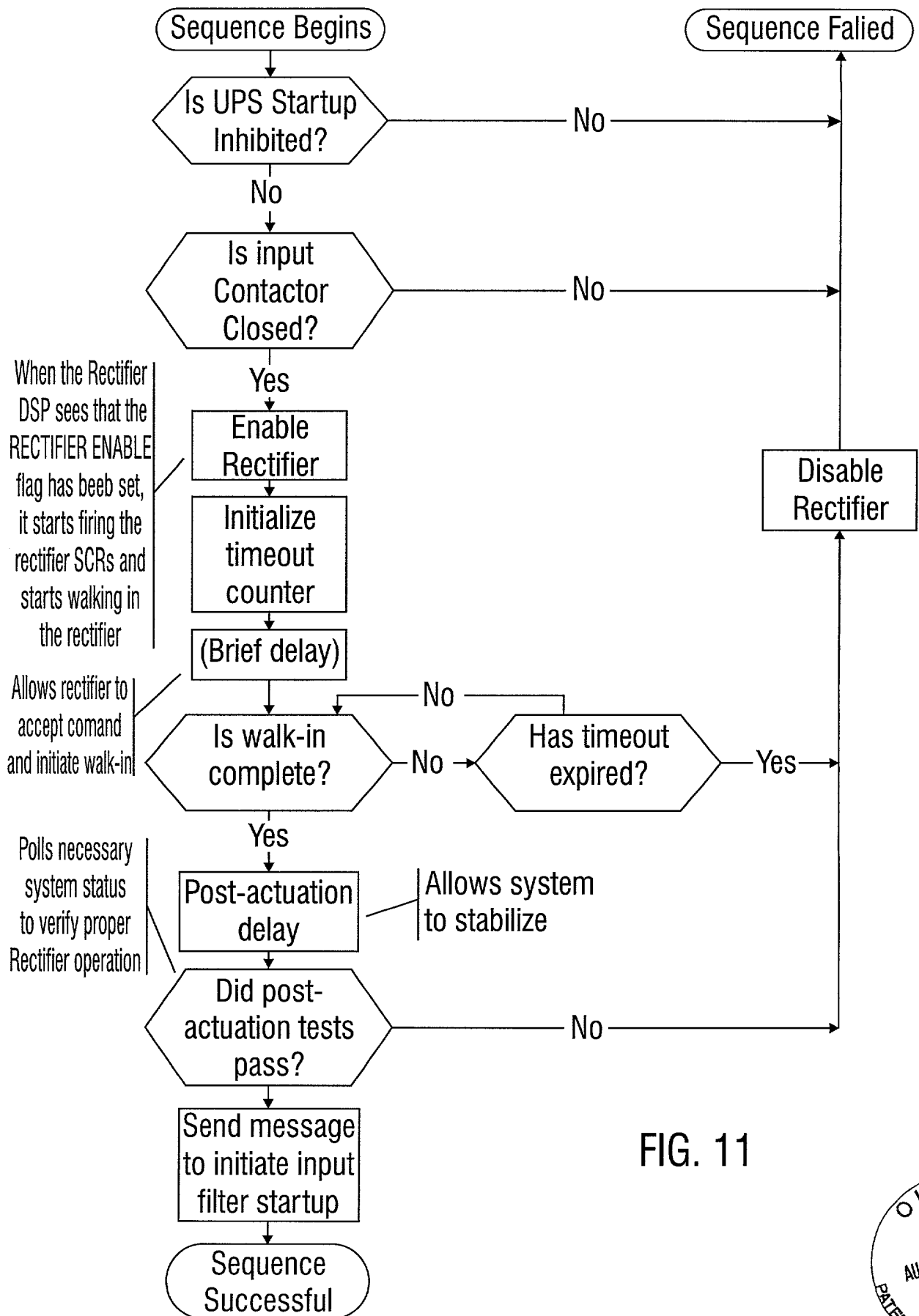
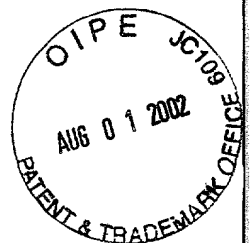


FIG. 11



2007-08-01 14:00:00

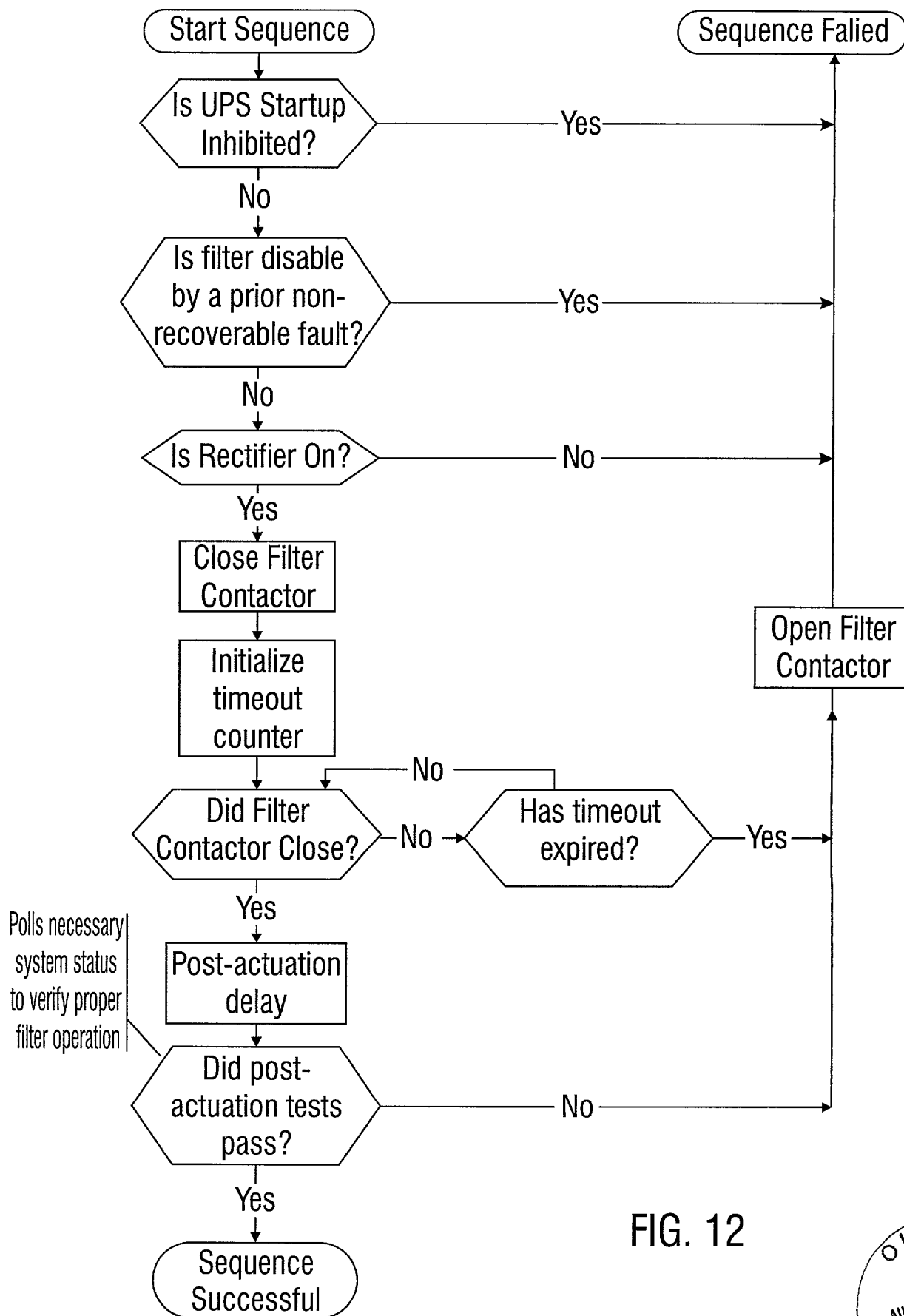


FIG. 12



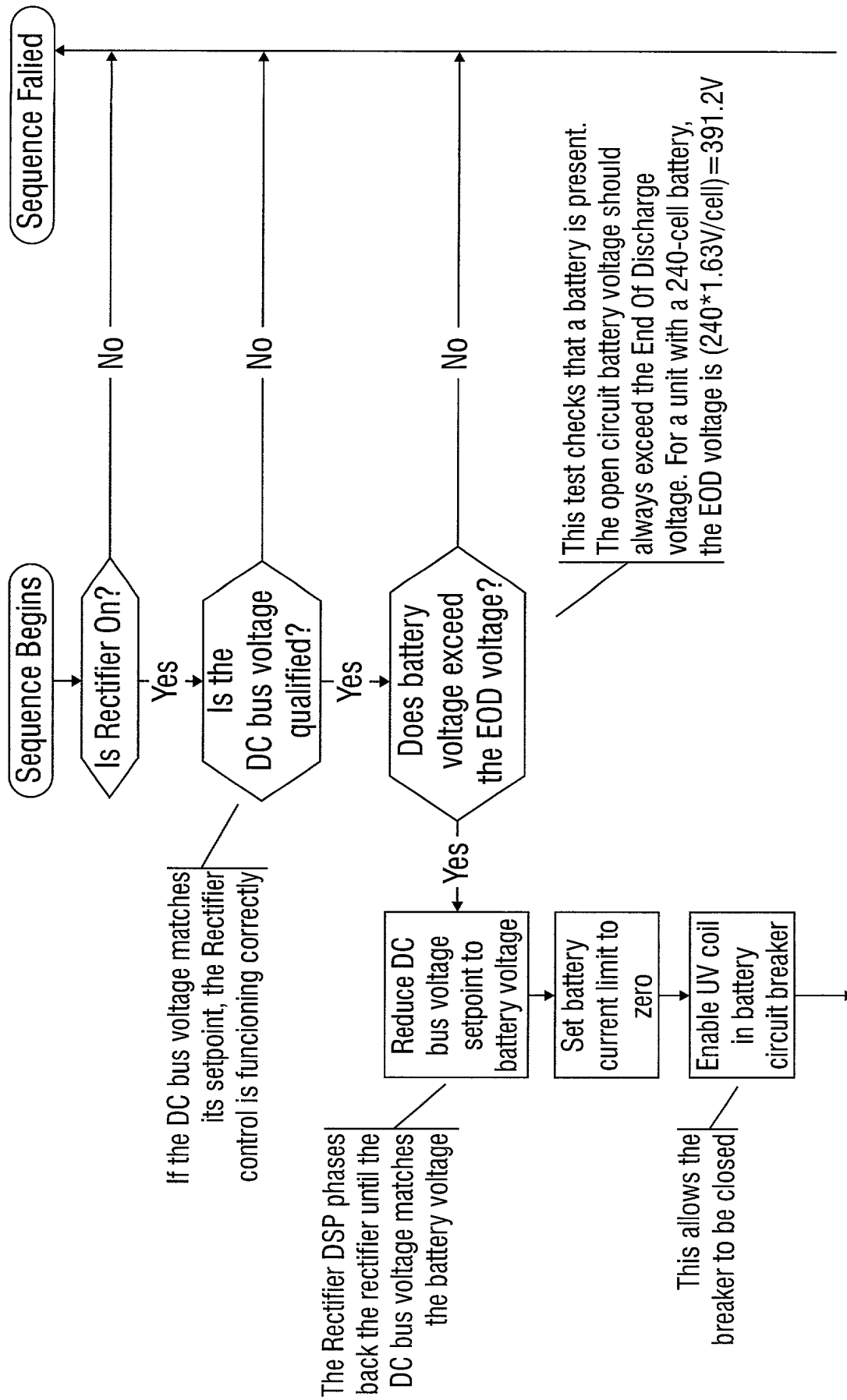


FIG. 14A







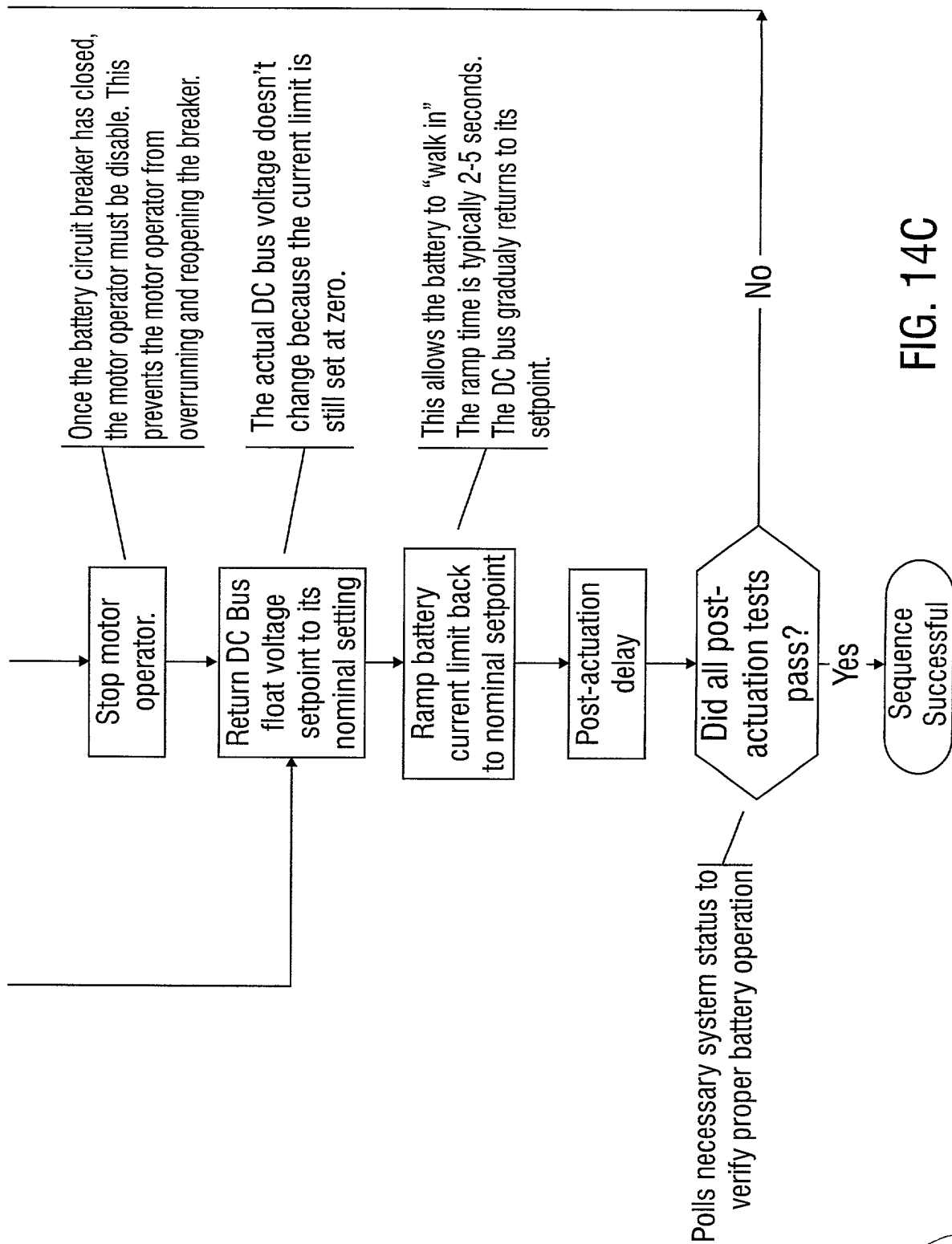


FIG. 14C

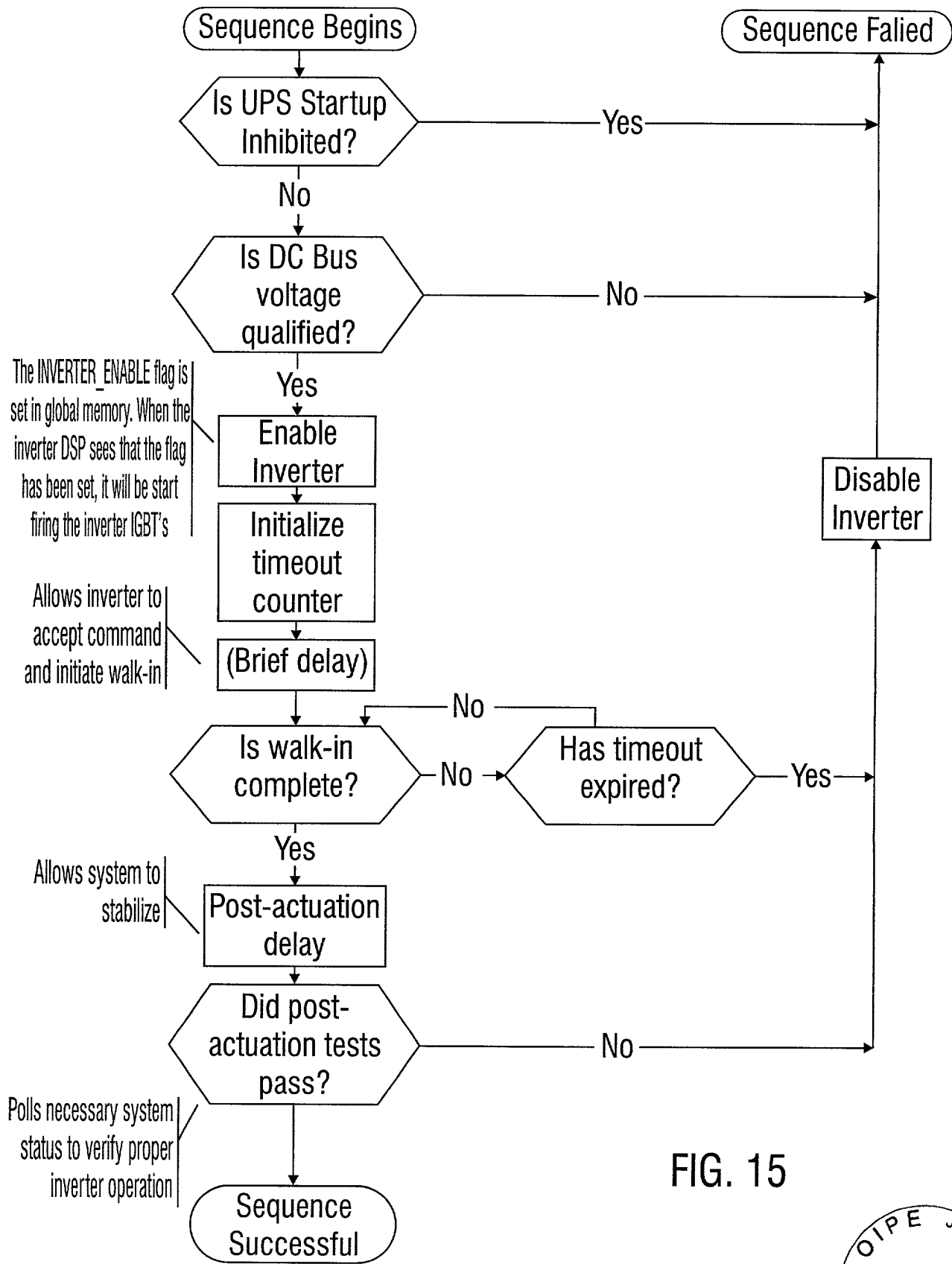
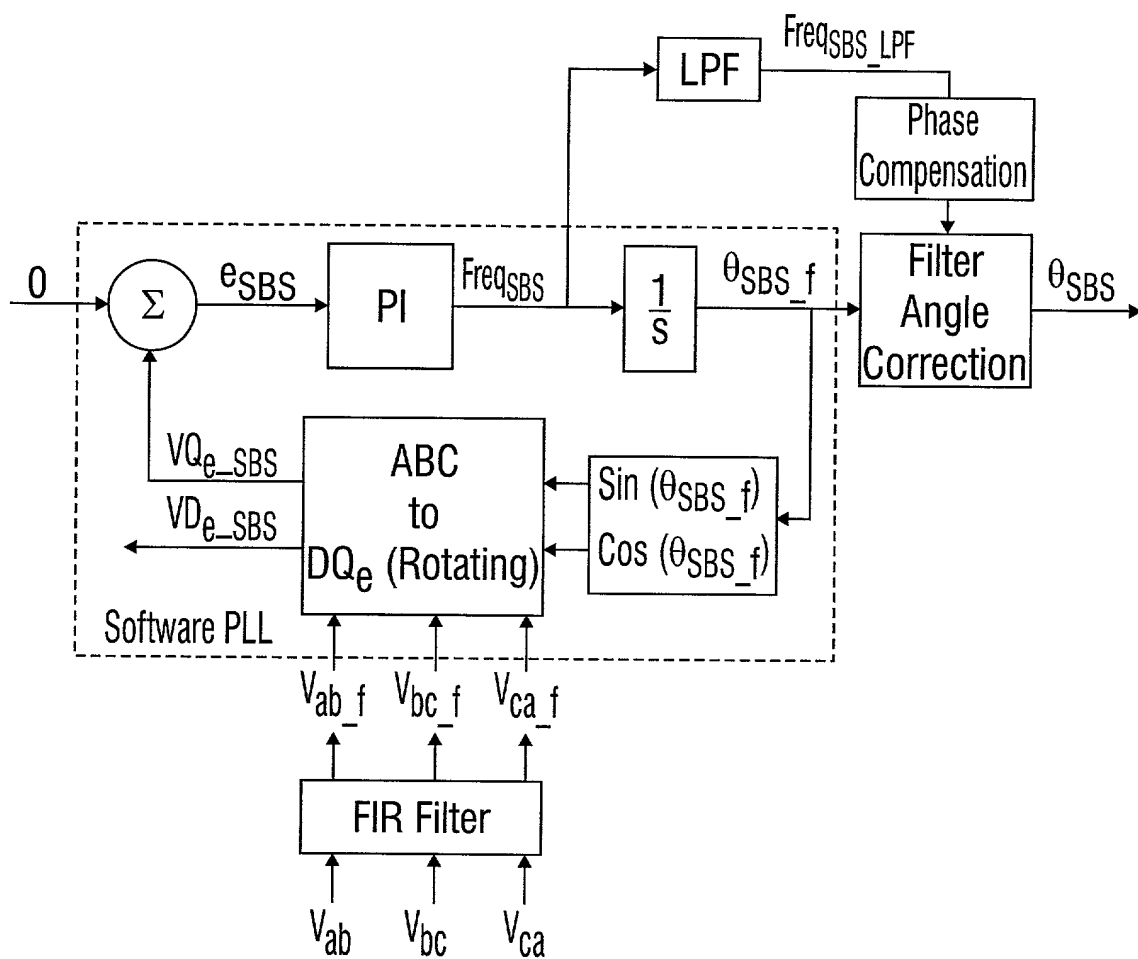


FIG. 15





Static Bypass Switch L-L Voltage

FIG. 16

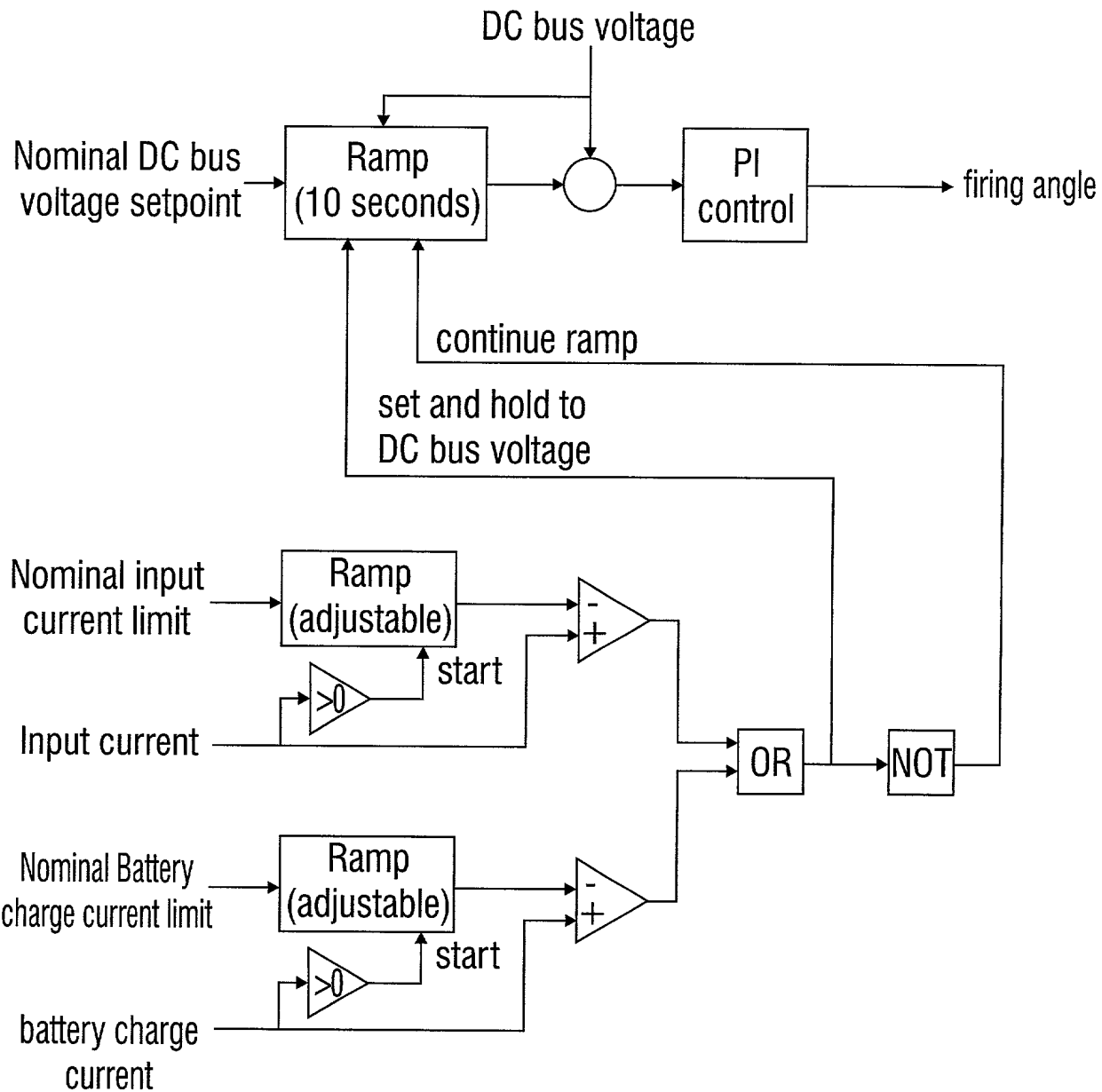


FIG. 17A

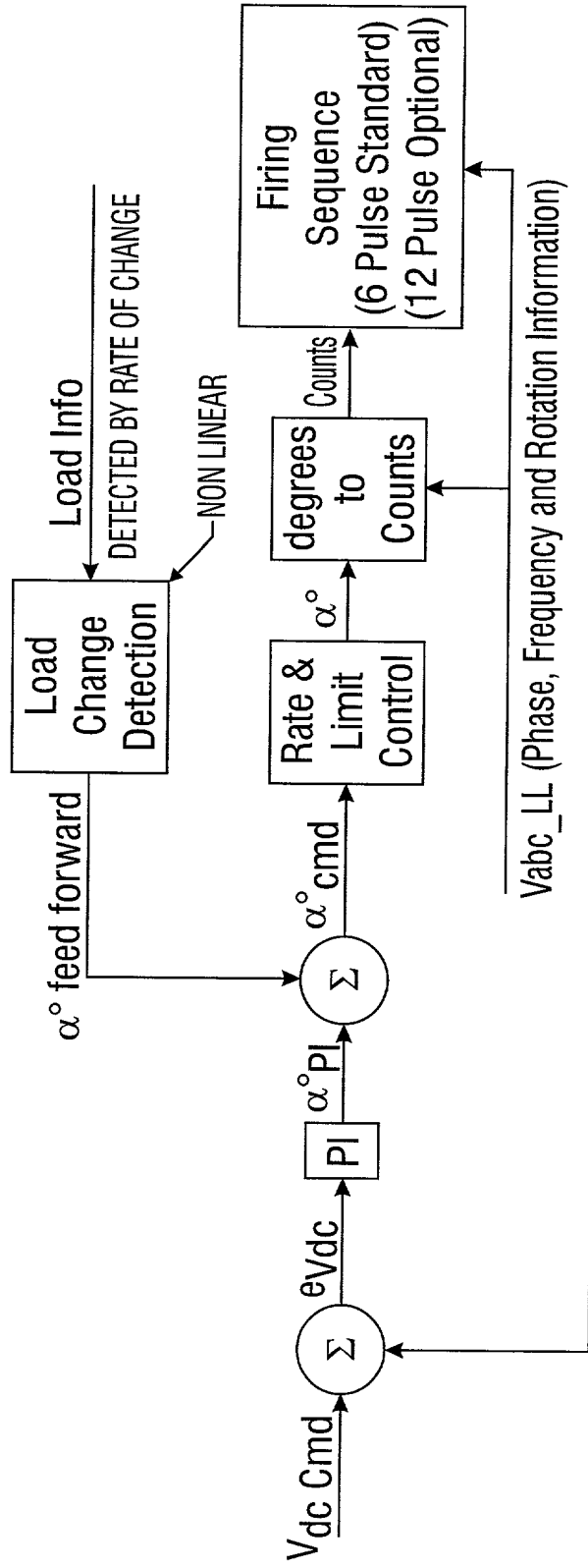


FIG. 17B



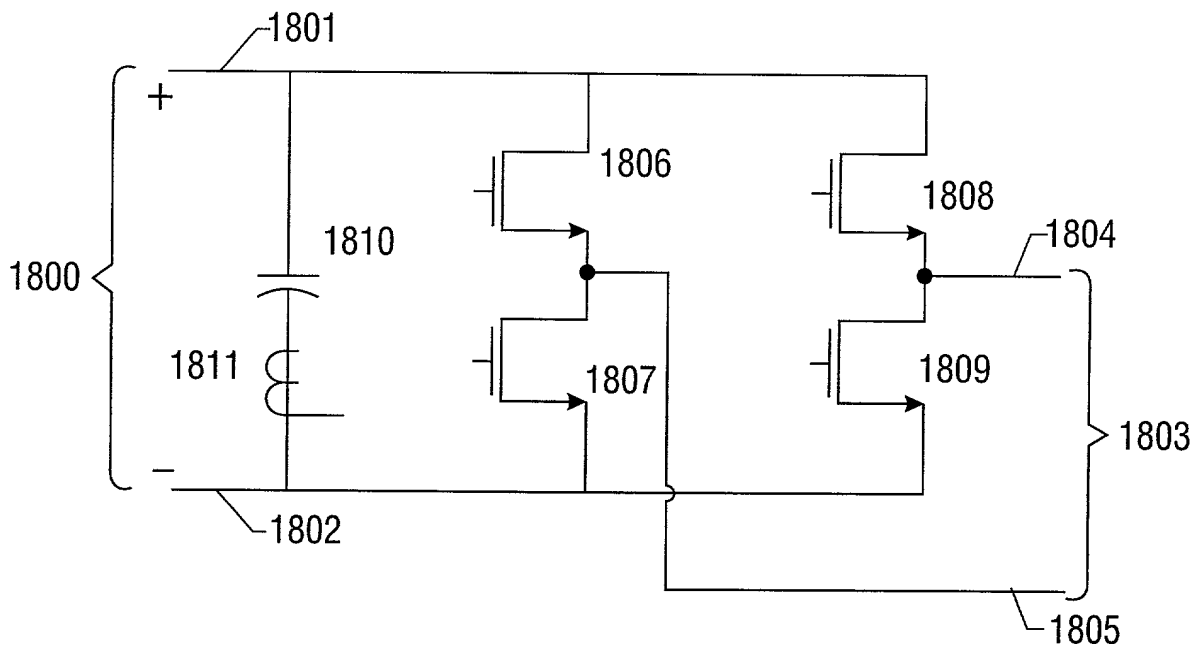


FIG. 18A

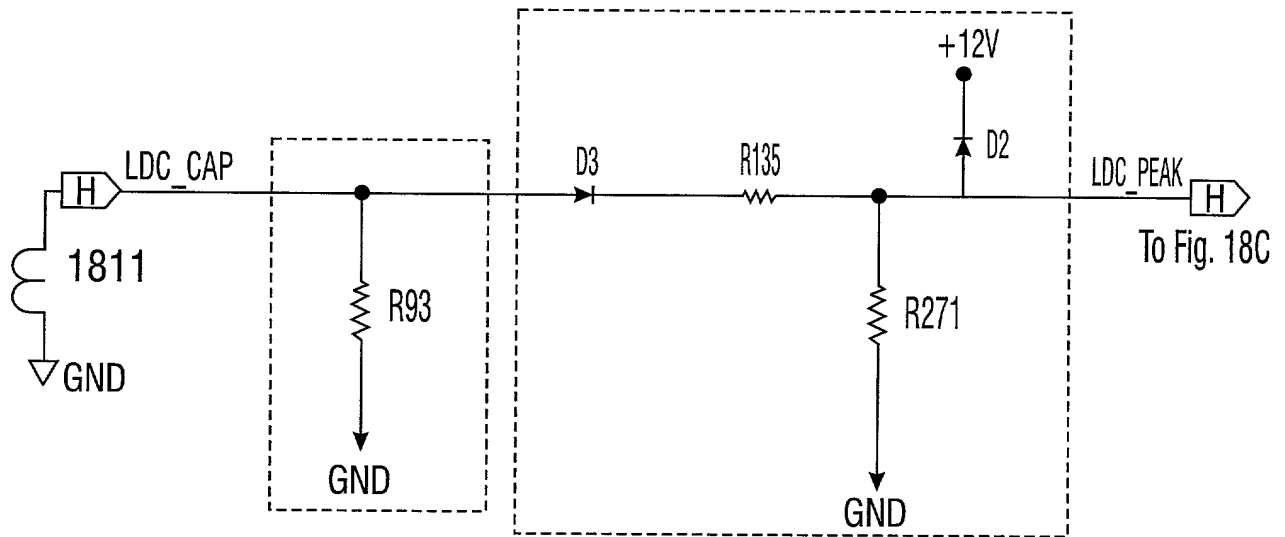


FIG. 18B





The diagram shows a three-phase inverter circuit. A split DC source, labeled 101, provides a positive voltage  $V_{DC}$  and a negative voltage  $-V_{DC}$ . The positive rail is connected to the gates of three upper MOSFETs: 102 ( $Q_{A+}$ ), 104 ( $Q_{B+}$ ), and 106 ( $Q_{C+}$ ). The negative rail is connected to the gates of three lower MOSFETs: 103 ( $Q_{A-}$ ), 105 ( $Q_{B-}$ ), and 107 ( $Q_{C-}$ ). The drains of the upper MOSFETs are connected to the positive rail, and the drains of the lower MOSFETs are connected to the negative rail. The sources of the upper MOSFETs are connected to the sources of the lower MOSFETs, forming three output lines labeled 108 (A), 109 (B), and 110 (C). Each output line has a solid dot at the connection point between the MOSFETs, indicating a neutral point or a specific connection point for a load.



Switch (0=OFF, i=ON)			Line to Neutral Voltage Vectors					Line to Line Voltage Vectors				
$S_C+$	$S_B+$	$S_A+$	$V_{AN}$	$V_{BN}$	$V_{CN}$	$V=[V_{QS} V_{DS}]^T$	Vector	$V_{AB}$	$V_{BC}$	$V_{CA}$	$V=[V_{QS} V_{DS}]^T$	Vector
0	0	1	$2/3 V_{dc}$	$-1/3 V_{dc}$	$-1/3 V_{dc}$	$2/3 V_{dc} \angle 0^\circ$	$\vec{V}_1$	$V_{dc}$	0	$-V_{dc}$	$2/\sqrt{3} V_{dc} \angle -30^\circ$	$\vec{V}_1$
1	0	1	$1/3 V_{dc}$	$-2/3 V_{dc}$	$1/3 V_{dc}$	$2/3 V_{dc} \angle 60^\circ$	$\vec{V}_2$	$V_{dc}$	$-V_{dc}$	0	$2/\sqrt{3} V_{dc} \angle 30^\circ$	$\vec{V}_2$
1	0	0	$-1/3 V_{dc}$	$-1/3 V_{dc}$	$2/3 V_{dc}$	$2/3 V_{dc} \angle 120^\circ$	$\vec{V}_3$	0	$-V_{dc}$	$V_{dc}$	$2/\sqrt{3} V_{dc} \angle 90^\circ$	$\vec{V}_3$
1	1	0	$-2/3 V_{dc}$	$1/3 V_{dc}$	$1/3 V_{dc}$	$2/3 V_{dc} \angle 180^\circ$	$\vec{V}_4$	$-V_{dc}$	0	$V_{dc}$	$2/\sqrt{3} V_{dc} \angle 150^\circ$	$\vec{V}_4$
0	1	0	$-1/3 V_{dc}$	$2/3 V_{dc}$	$-1/3 V_{dc}$	$2/3 V_{dc} \angle 240^\circ$	$\vec{V}_5$	$-V_{dc}$	$V_{dc}$	0	$2/\sqrt{3} V_{dc} \angle 210^\circ$	$\vec{V}_5$
0	1	1	$1/3 V_{dc}$	$1/3 V_{dc}$	$-2/3 V_{dc}$	$2/3 V_{dc} \angle 300^\circ$	$\vec{V}_6$	0	$V_{dc}$	$-V_{dc}$	$2/\sqrt{3} V_{dc} \angle 270^\circ$	$\vec{V}_6$
0	0	0	0	0	0	0	$\vec{V}_7$	0	0	0	0	$\vec{V}_7$
1	1	1	0	0	0	0	$\vec{V}_8$	0	0	0	0	$\vec{V}_8$

FIG. 20



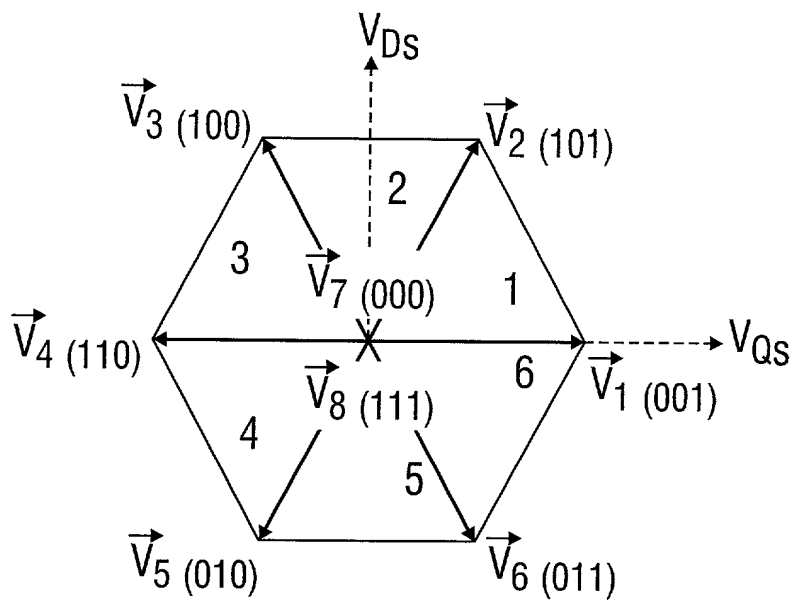


FIG. 21A

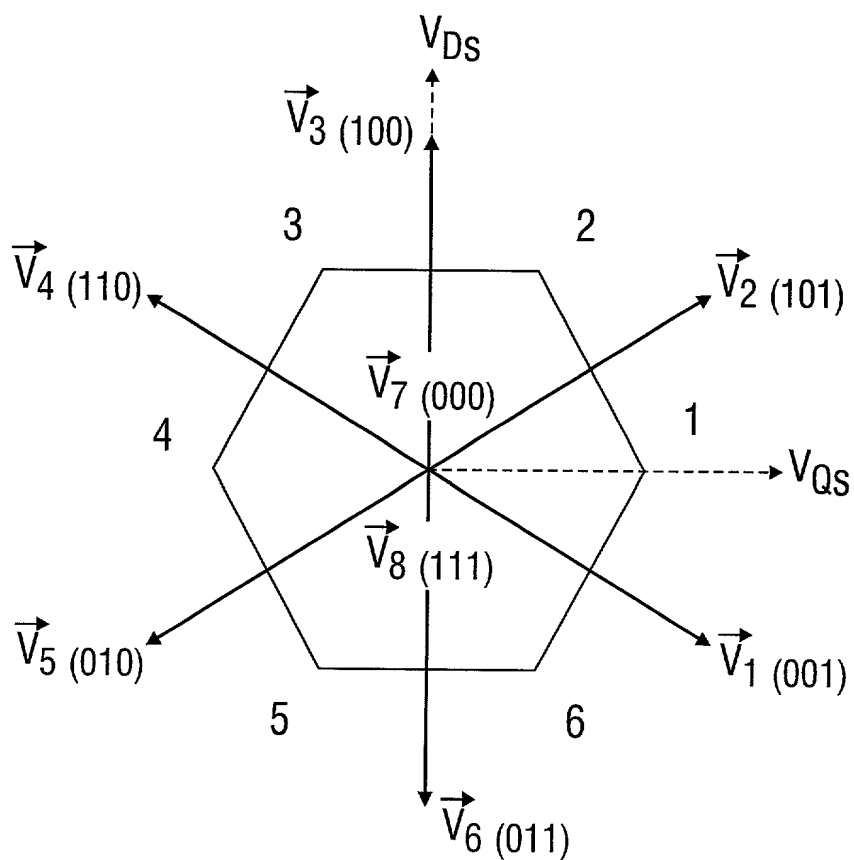


FIG. 21B



2007-03-01 14:00:00

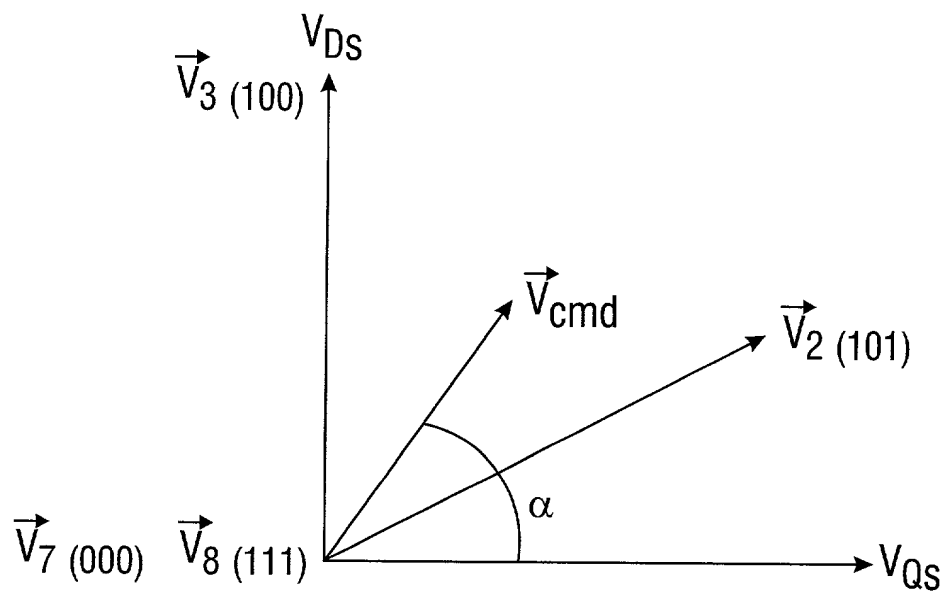


FIG. 22A

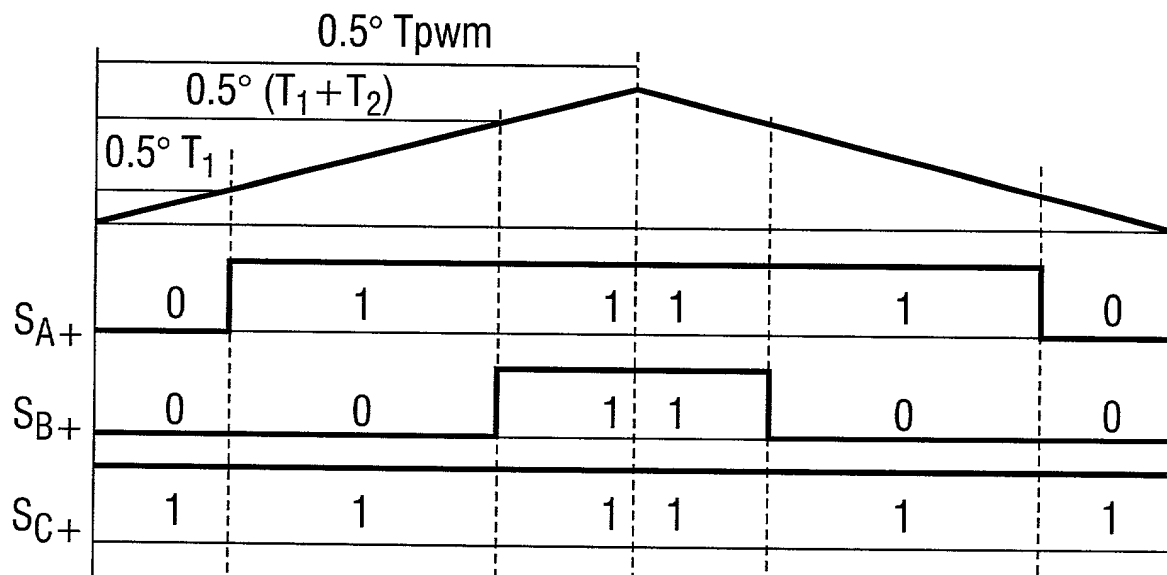


FIG. 22B



2007-03-24 14:00:00

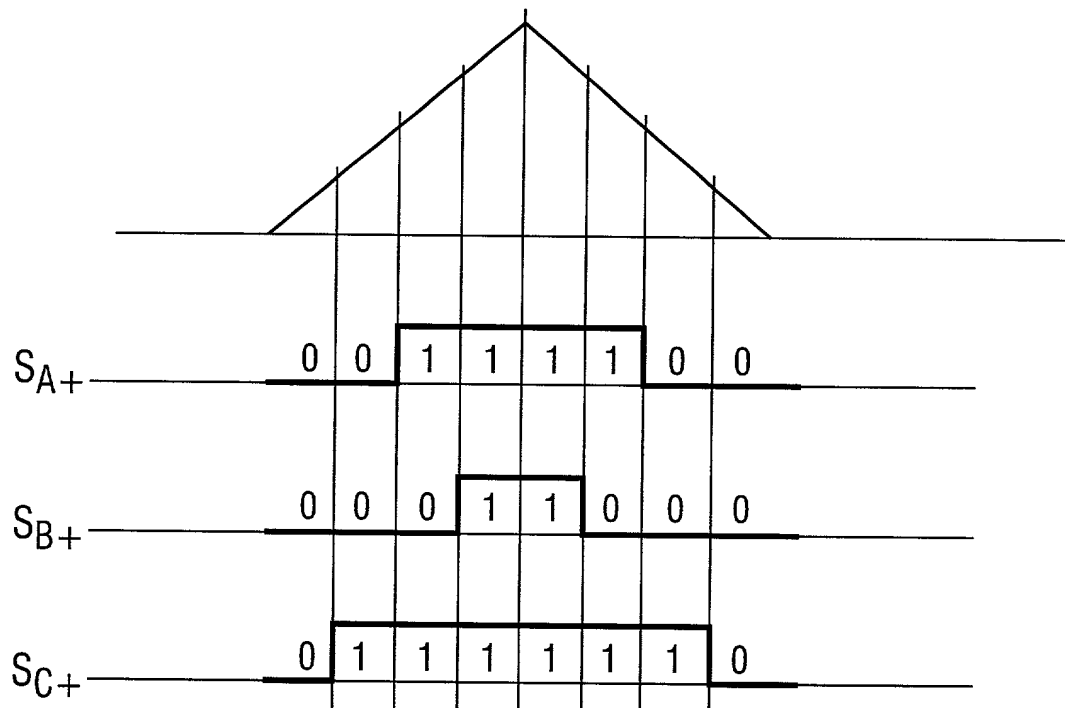


FIG. 22C



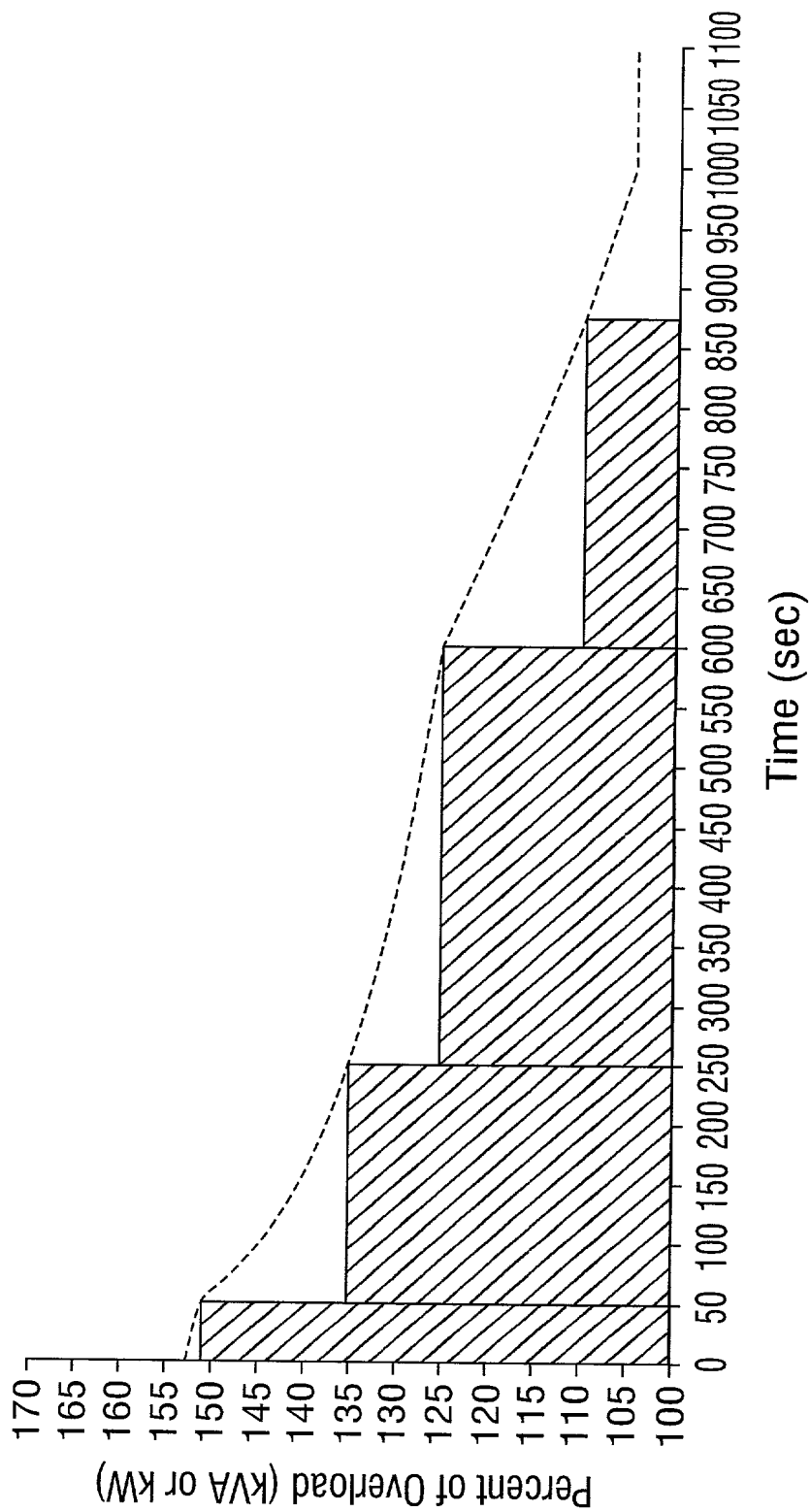


FIG. 23



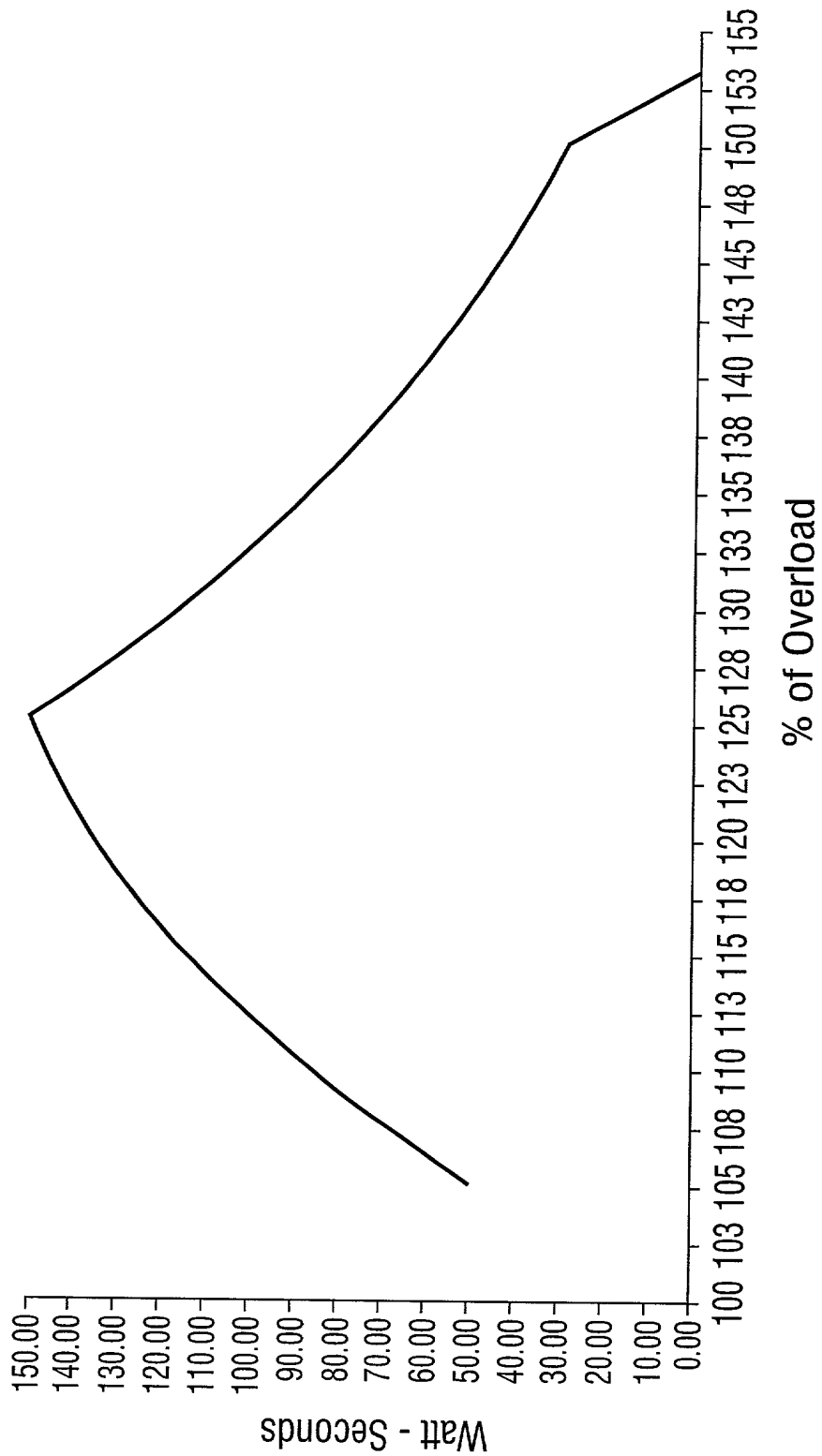


FIG. 24











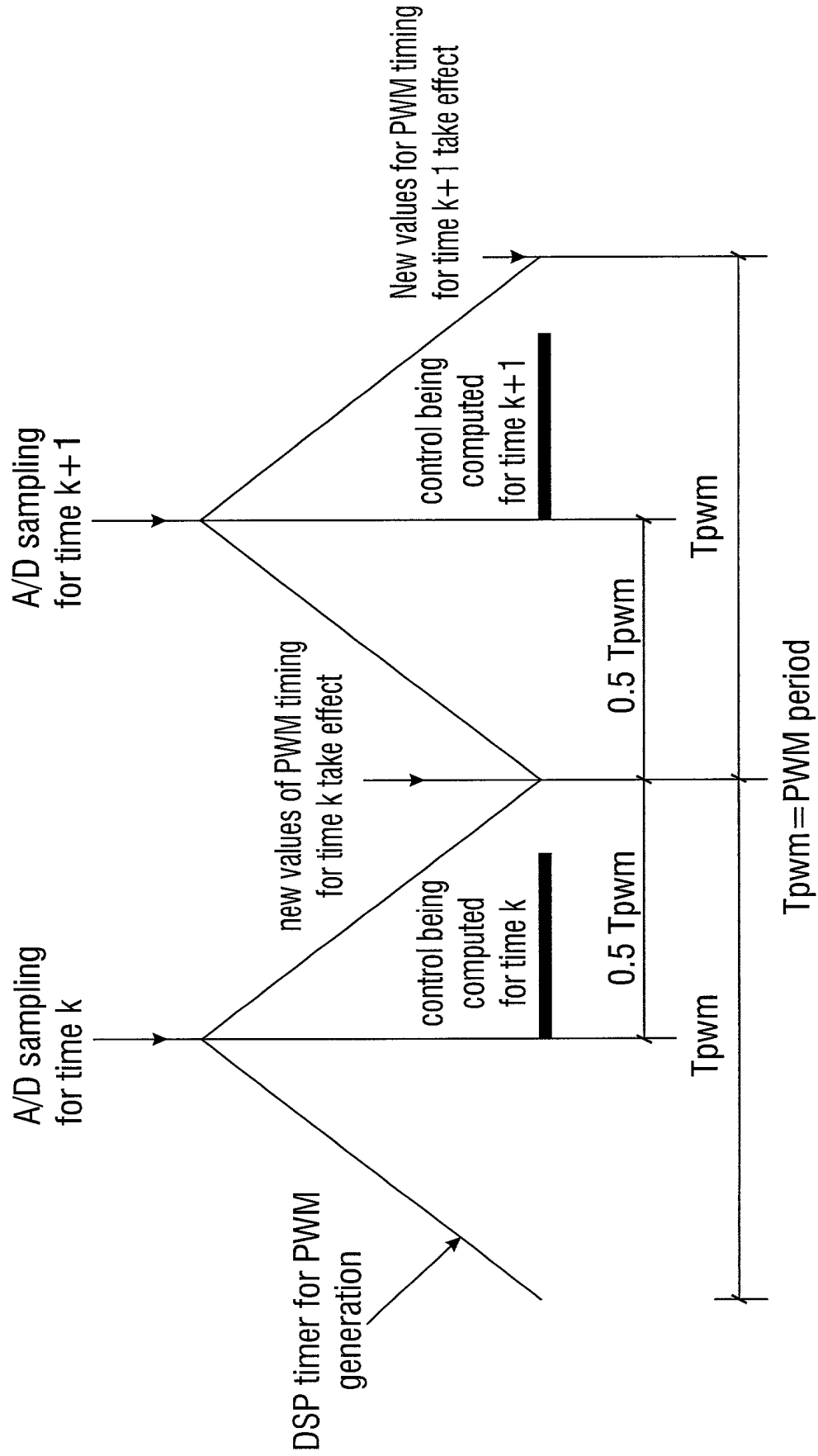


FIG. 29



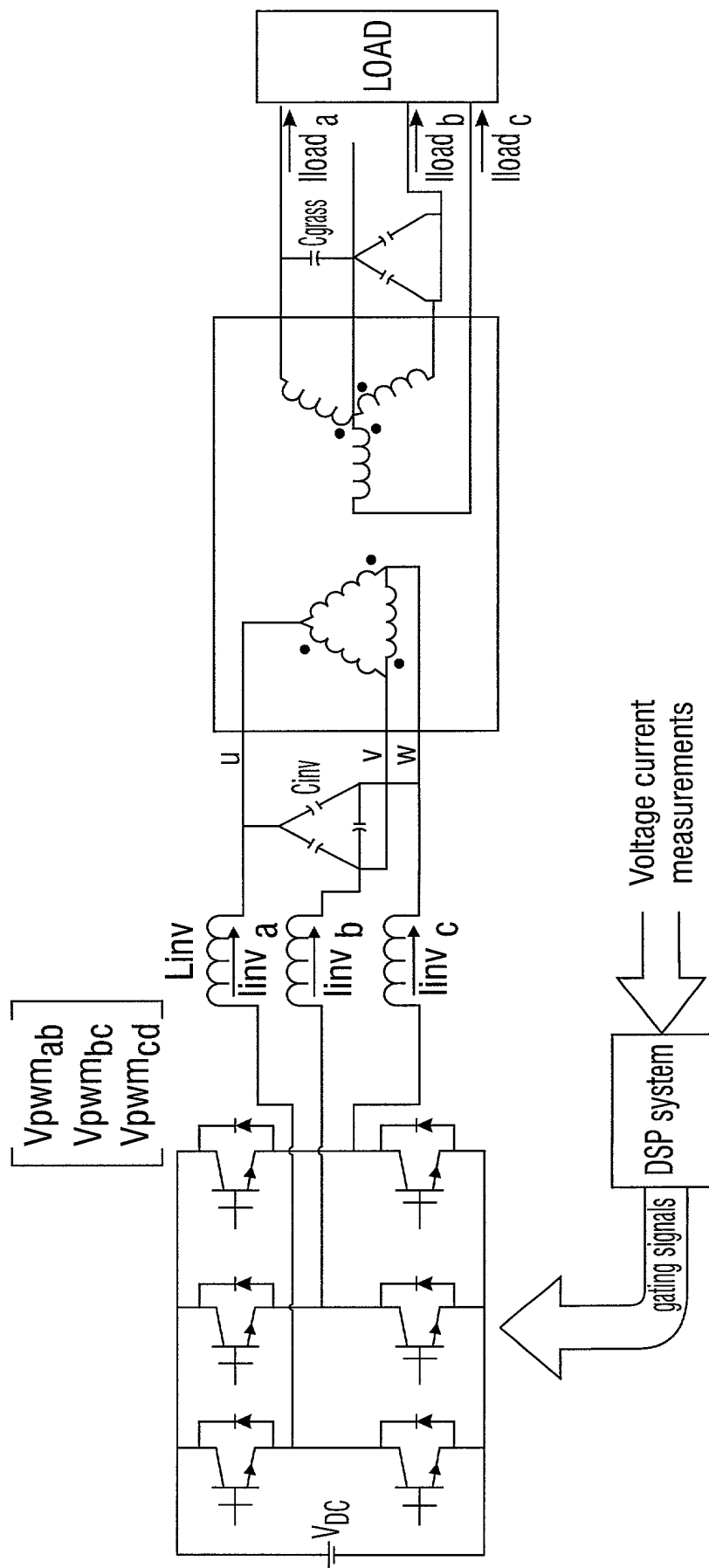


FIG. 30

## DELTA-WYE TRANSFORMER

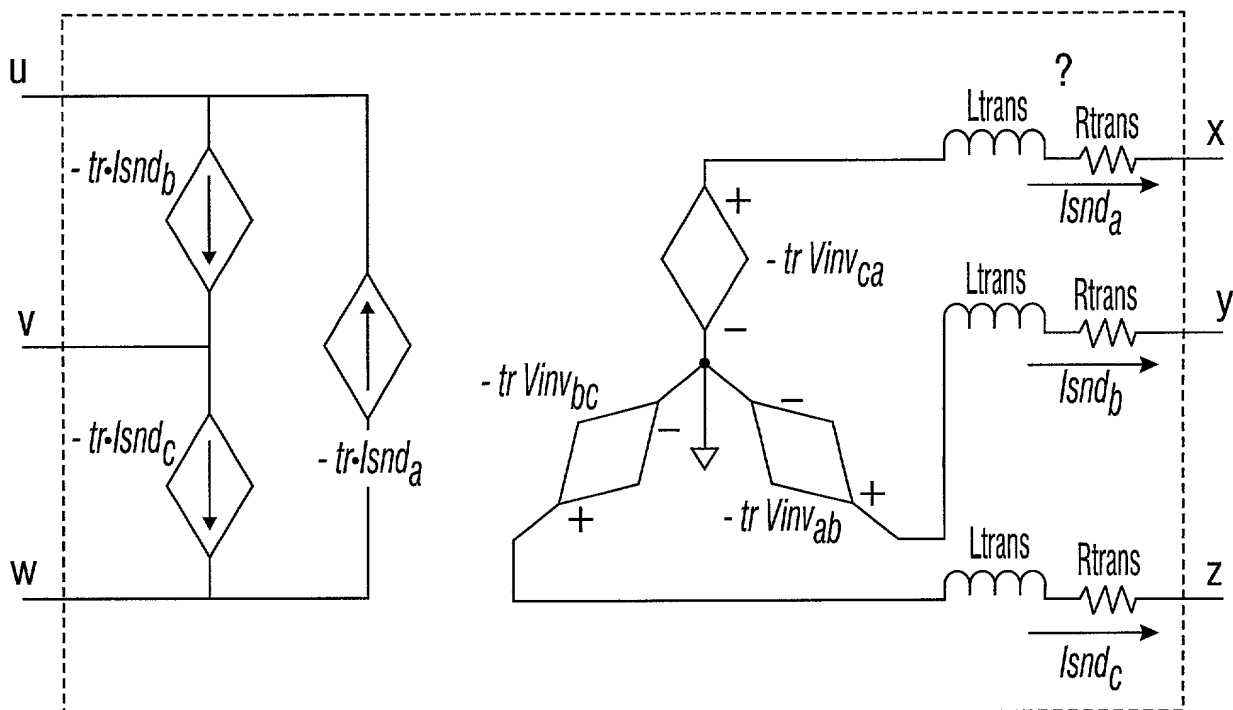


FIG. 31



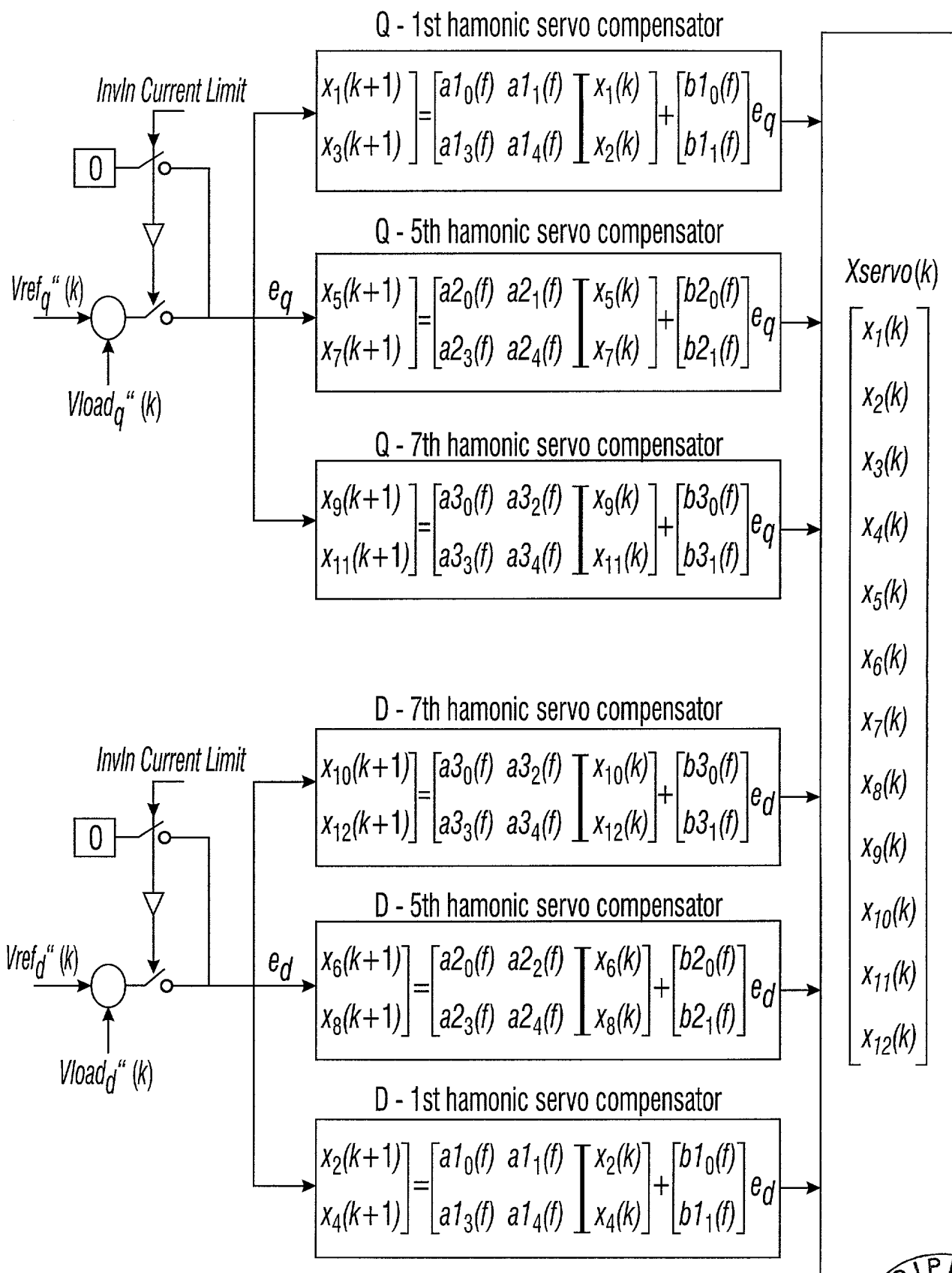
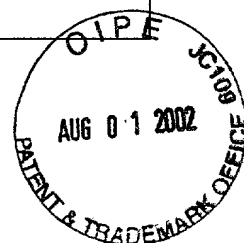


FIG. 32



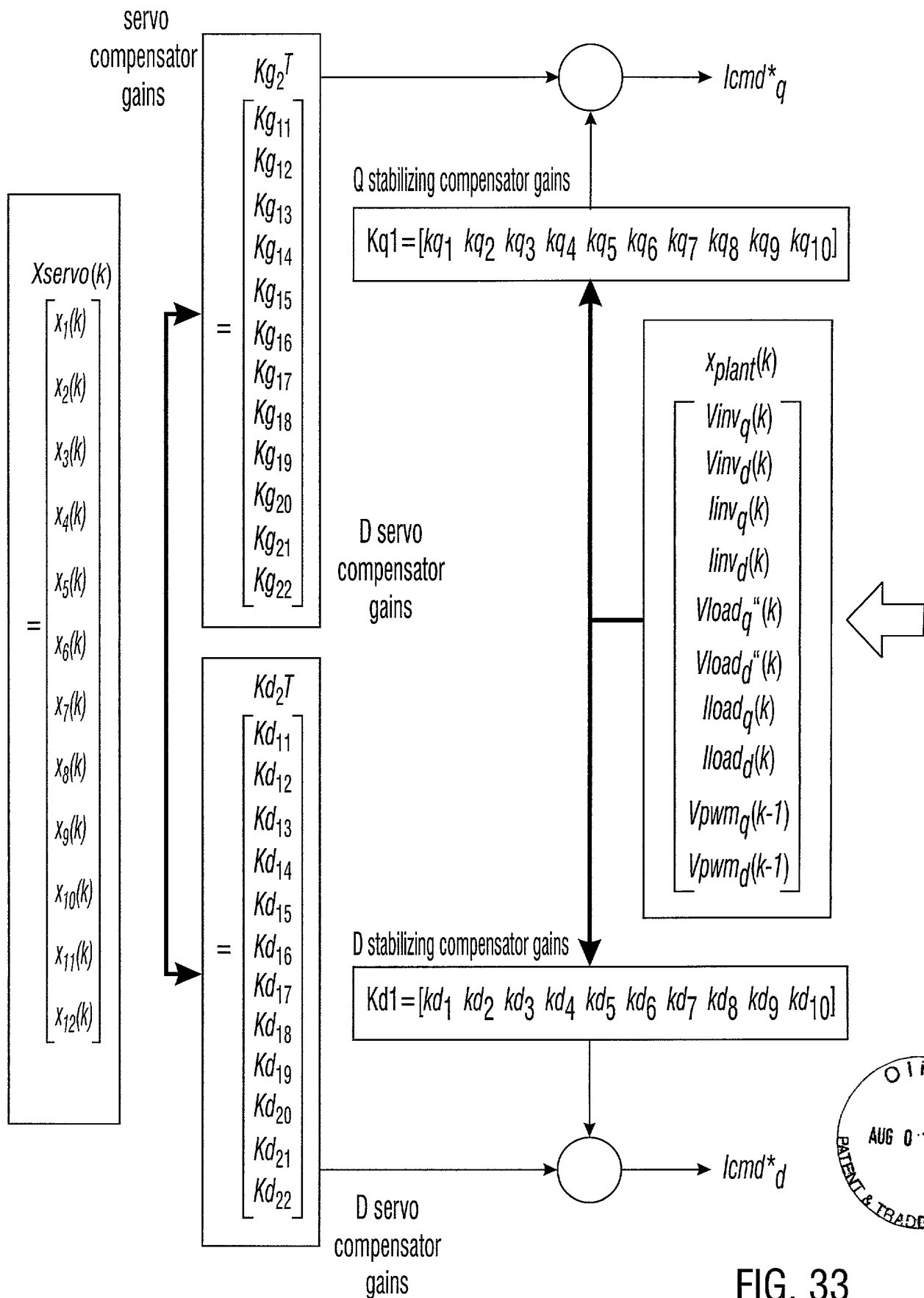


FIG. 33

FIG. 35A-1	FIG. 35A-2	FIG. 35A-5
FIG. 35A-3	FIG. 35A-4	
FIG. 35A-6	FIG. 35A-7	

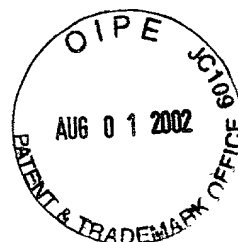


FIG. 35A

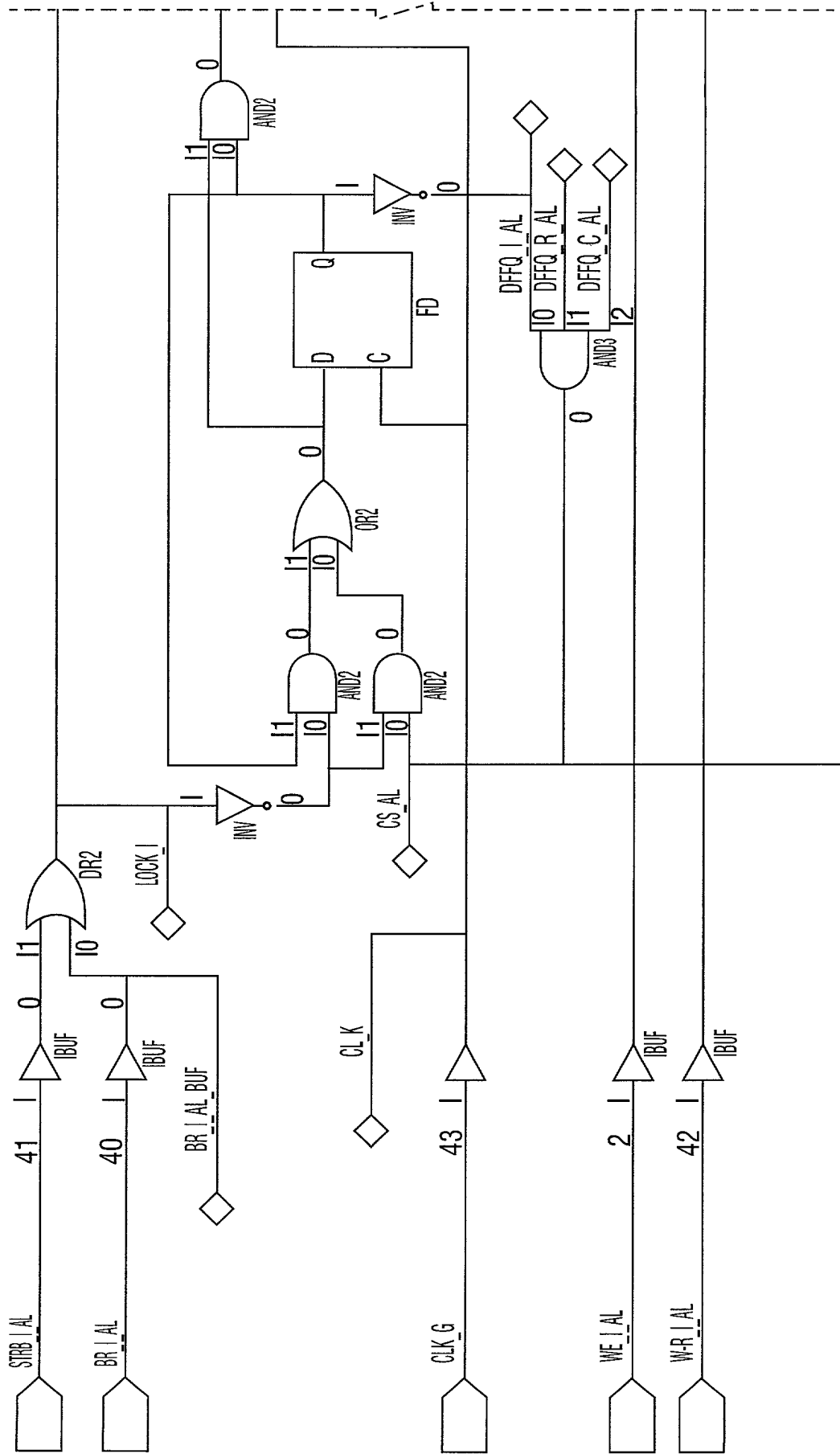


FIG. 35A-1





[illegible]

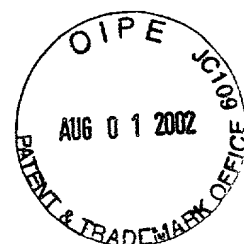
The logic diagram shows a 2-bit register. It has two 2-to-1 multiplexers (MUX) at the input, each with a select line (S0 and S1) and two data inputs (I0 and I1). The MUX outputs are connected to the D inputs of a D flip-flop (FD). The flip-flop has a clock input (CLK) and a feedback loop from its Q output to its D input. The output of the flip-flop is connected to a 2-to-1 MUX at the output, which has a select line (S2) and two data inputs (O0 and O1). The output of the MUX is connected to the Q output of the flip-flop. The diagram also shows a 2-to-1 MUX at the input of the flip-flop, which has a select line (S0) and two data inputs (I0 and I1). The output of this MUX is connected to the D input of the flip-flop. The flip-flop has a clock input (CLK) and a feedback loop from its Q output to its D input. The output of the flip-flop is connected to a 2-to-1 MUX at the output, which has a select line (S2) and two data inputs (O0 and O1). The output of the MUX is connected to the Q output of the flip-flop.

**FIG. 35A-3**



[illegible]

**FIG. 35A-4**





2  
JC100 OFFICE 69



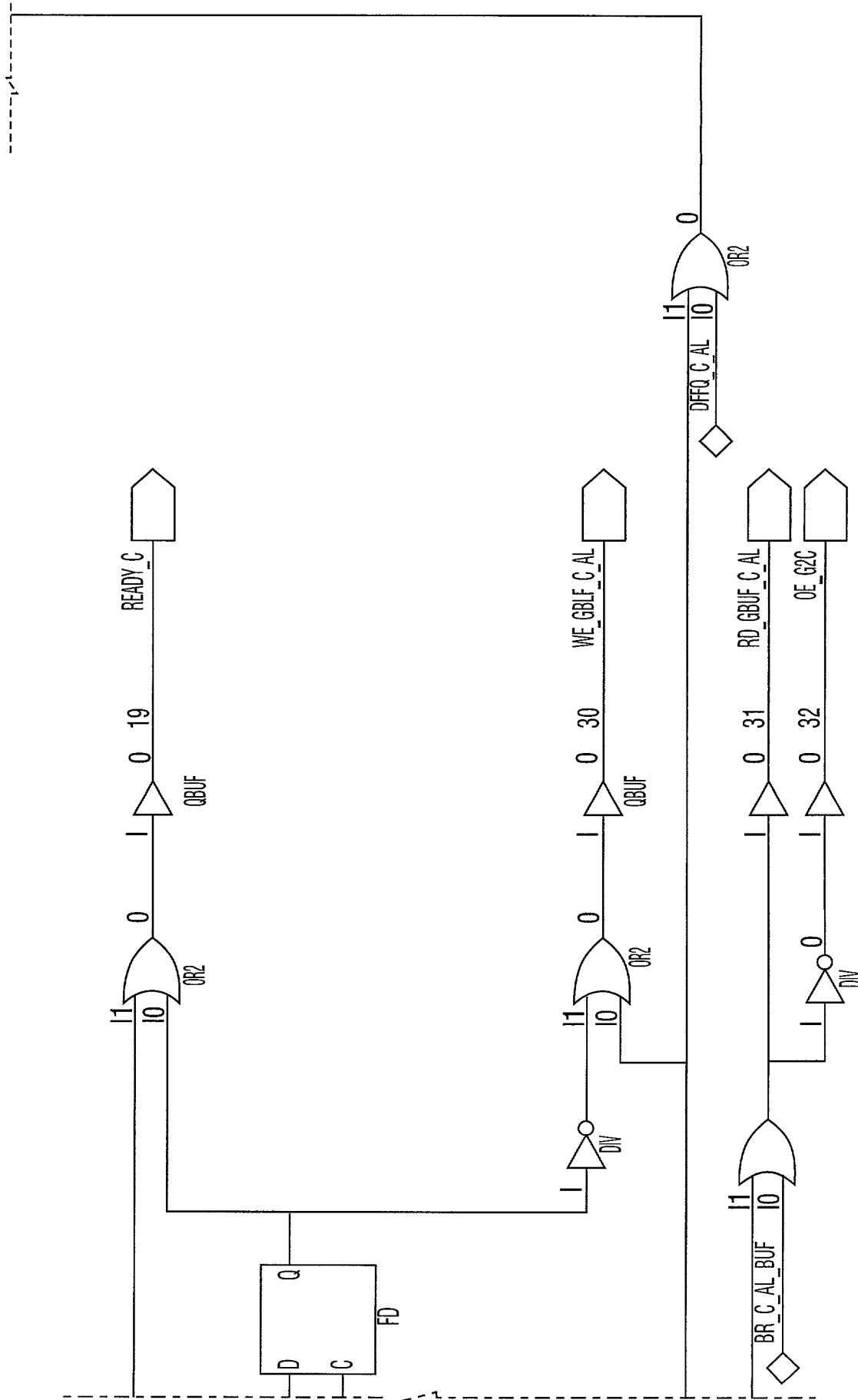


FIG. 35A-7



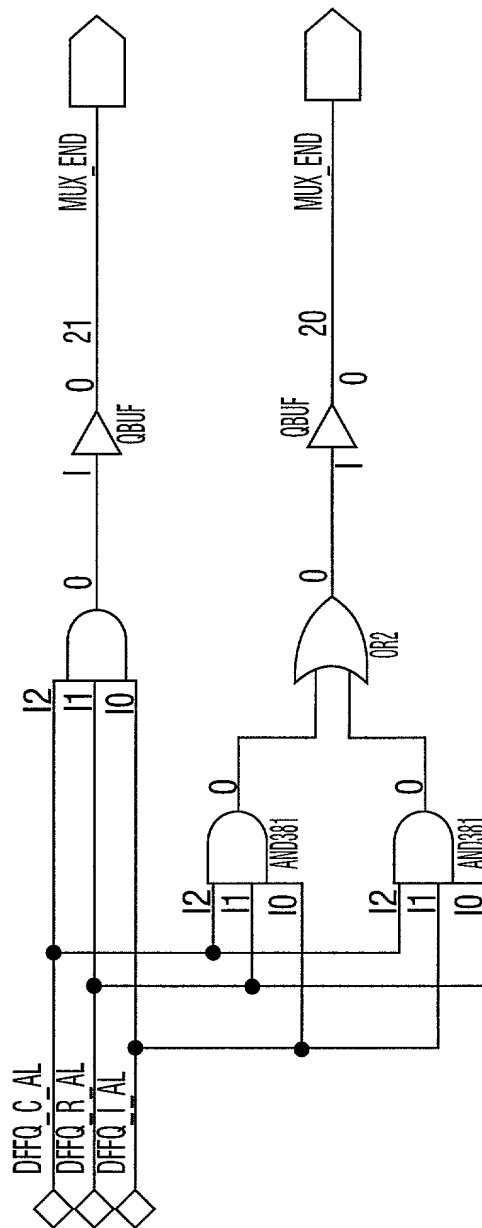


FIG. 35B

```
sequenceDiagram
    participant T as Transmitter Node
    participant R as Receiver Node
    Note over T: Time out
    T->>R: Fragment Msg. 1
    R-->T: Fragment Msg. 1, ack(Pass)
    T->>R: Fragment Msg. 2
    R-->T: Fragment Msg. 2, Ack(Pass)
    T->>R: Fragment Msg. 3
    R-->T: Fragment Msg. 3, Ack(Pass)
    T->>R: Fragment Msg. N
    R-->T: Fragment Msg. N, Ack(Pass)
```



2007-07-20 10:00:00

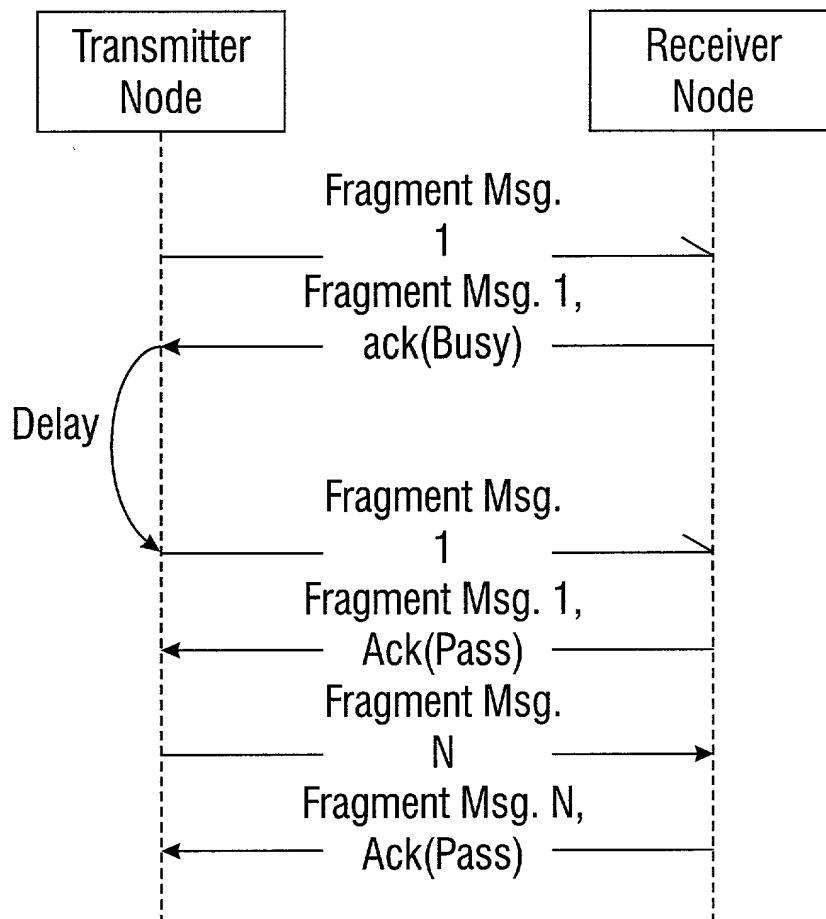
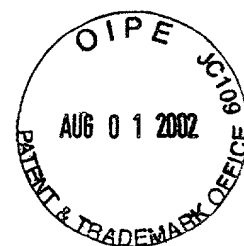


FIG. 37



2002-08-01

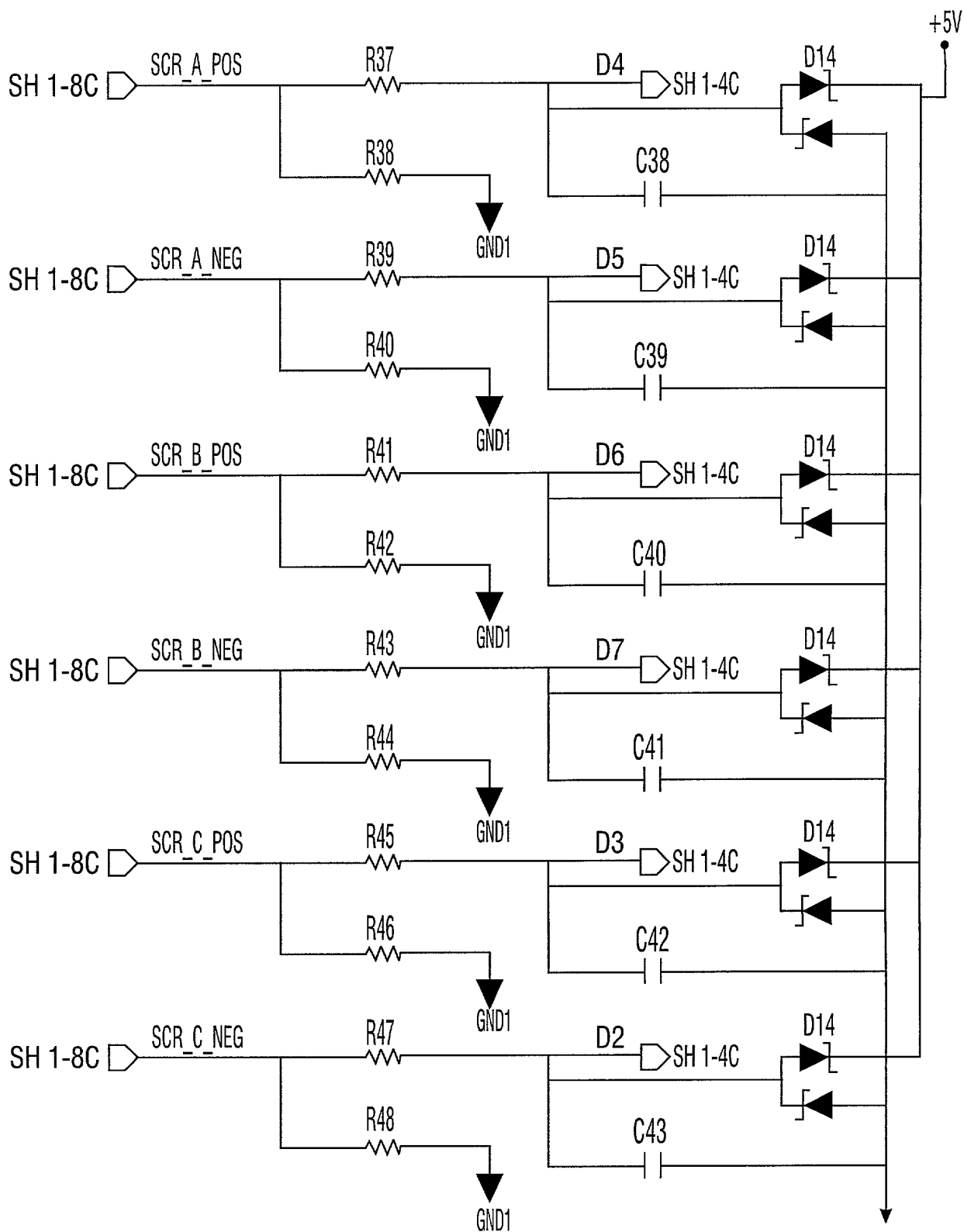
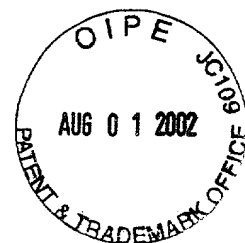


FIG. 38A



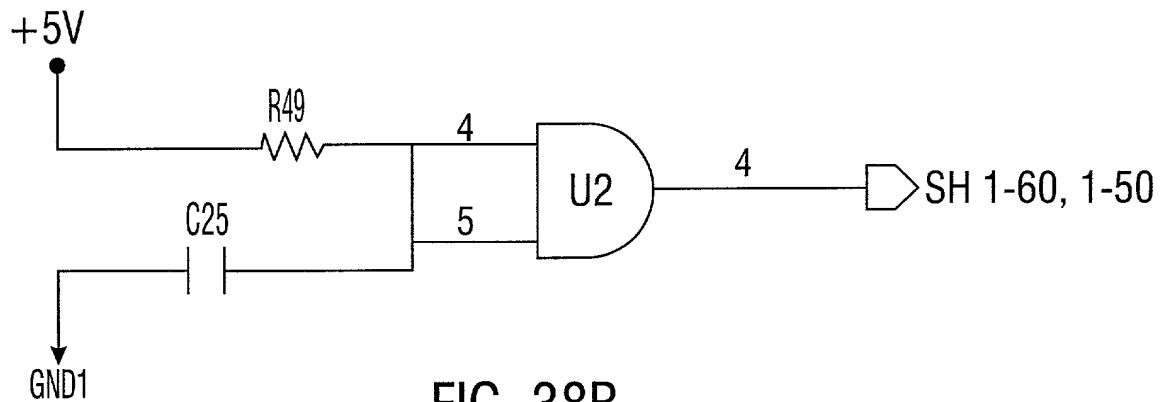


FIG. 38B

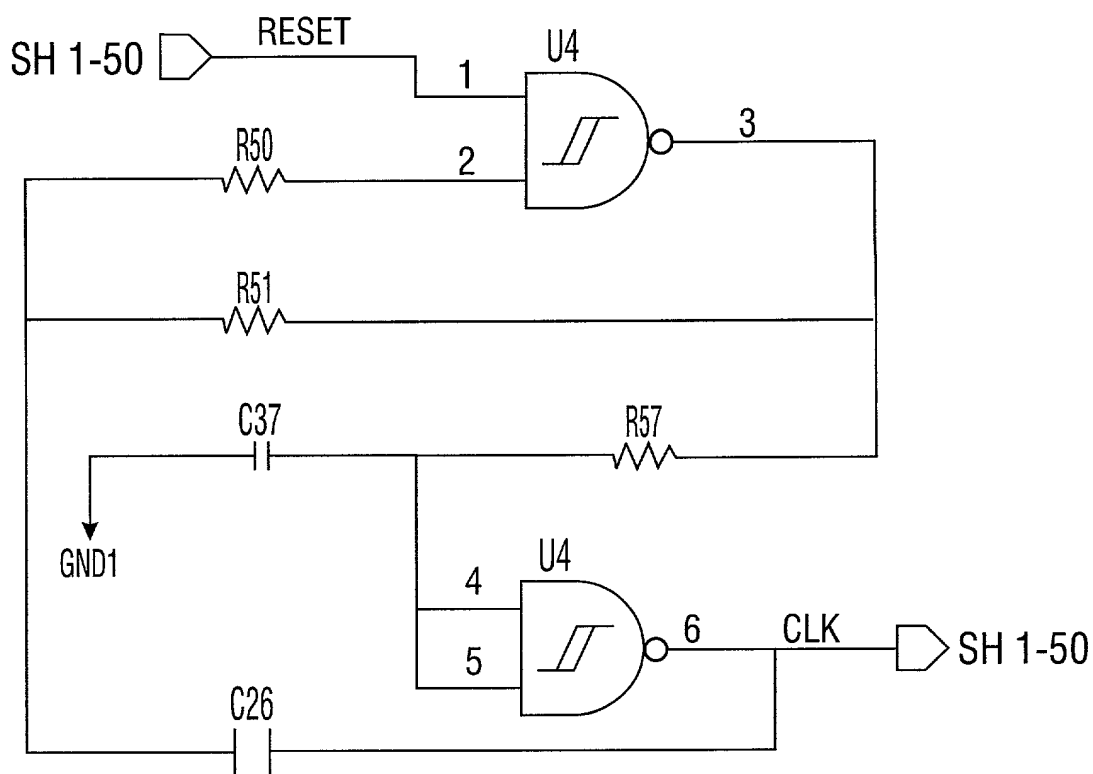
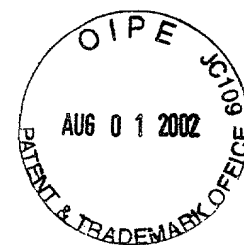
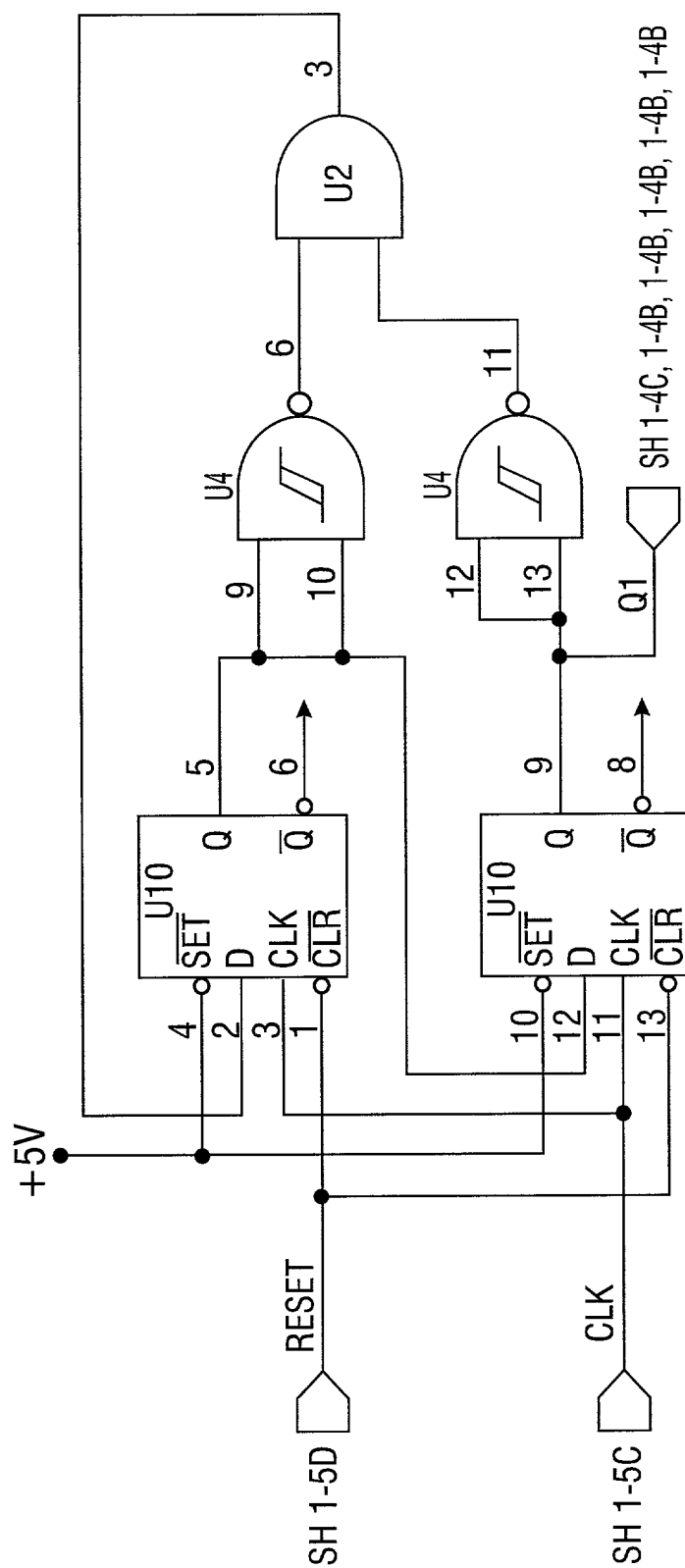


FIG. 38C









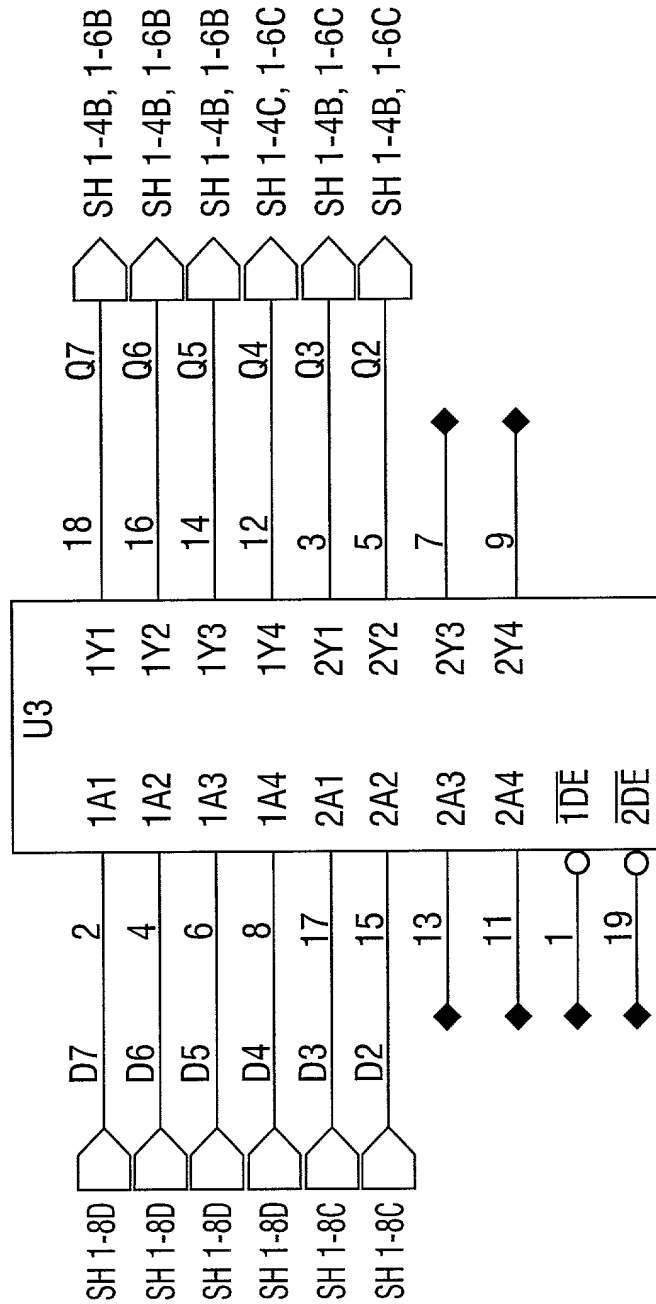


FIG. 38G

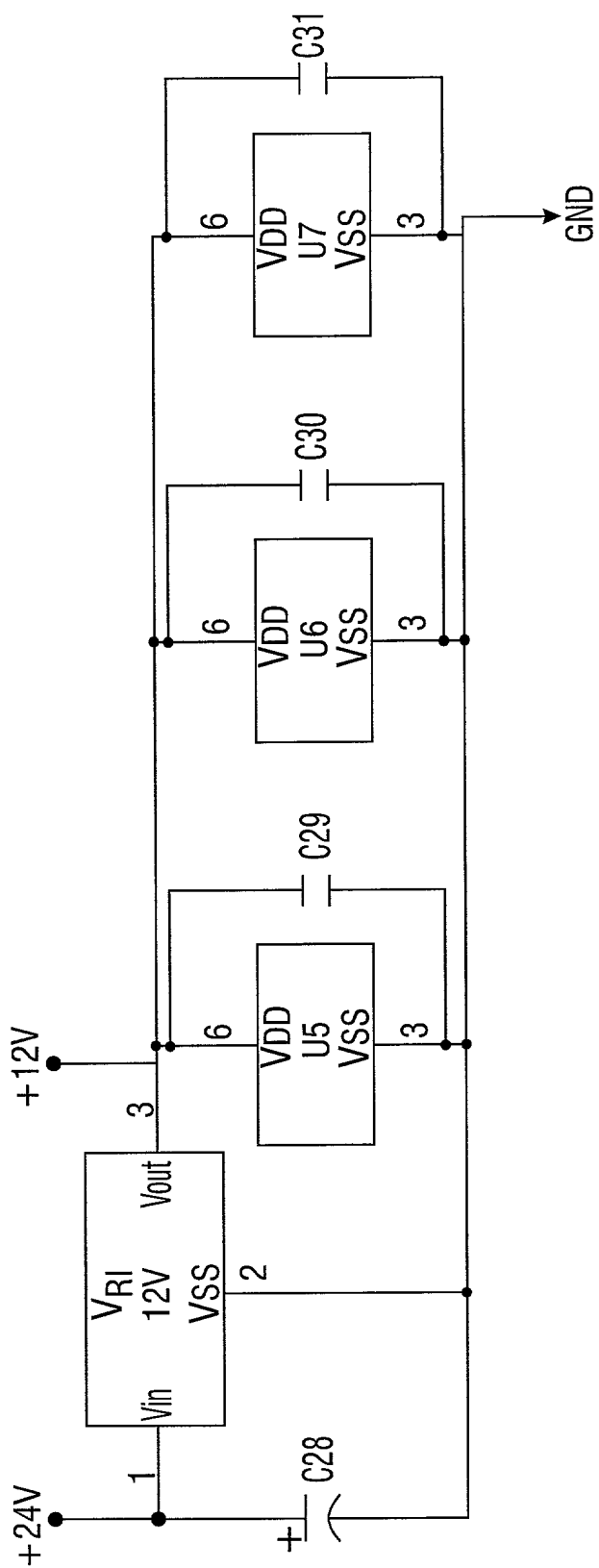


FIG. 38H







